Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 12, No. 2, December : 2023

FOUR-LEVEL THREE-PHASE INVERTER WITH REDUCED COMPONENT COUNT FOR LOW AND MEDIUM VOLTAGE APPLICATIONS

V Sree Lakshmi, PG Scholar, Dept of EEE, JNTUA CEA, Ananthapuramu, Andhra Pradesh, India. :
J Suresh, Research Scholar, Dept of EEE, JNTUA CEA, Ananthapuramu, Andhra Pradesh, India. :
Dr R Kiranmayi, Professor, Dept of EEE, JNTUA CEA, Ananthapuramu, Andhra Pradesh, India. :
veerapureddysreelakshmi6@gmail.com ; Suresh55j@yahoo.co.in; kiranmayi0109@gmail.com

ABSTRACT

This paper proposes a novel three-phase topology with a reduced component count for low and medium-voltage systems. It requires three bidirectional switches and twelve unidirectional switches for producing four-level voltages without using flying capacitors or clamping diodes, reducing the size, cost, and losses. Removing flying capacitors and clamping diodes allows it to simplify control algorithms and increase the reliability, efficiency, and lifetime. A modified low-frequency modulation (LFM) scheme is developed and implemented on the proposed topology to produce a staircase voltage with four steps. Further, a level-shifted pulse width modulation (LSPWM) is used to reduce the filter size and increase the output voltage controllability. In this study, a voltage balancing control algorithm is executed to balance the DC-link capacitor voltages. The performance of the proposed topology is numerically demonstrated and experimentally validated on an in-house test setup. Within the framework, the power loss distribution in switches and conversion efficiency of the proposed circuit are studied, and its main features are highlighted through a comparative study.

I. INTRODUCTION

Multilevel inverters (MLIs) have gained popularity in DC-AC converters, with a wide range of voltage levels, due to their attractive features of low harmonic contents, low dv/dt voltage stress, low filtering requirements, low switching frequency, and using low-rated semiconductor devices. Further, some MLIs have a modularity feature, enabling transformer less operation and increasing the reachable output voltage without increasing the semiconductor device rating [1]–[5]. These unique features make the MLIs remarkable among other DC-AC converters. The cascaded H-bridge MLI (CHB-MLI) [6], neutral-point clamped MLI (NPC-MLI) [7], [8], and flying capacitor MLI (FC-MLI) [9], [10] are considered as the baseline topologies of MLIs. On the other hand, producing a higher count of voltage levels dramatically increases the counts of clamping diodes, flying capacitors, and isolated DC sources NPC-MLI, FC-MLI, and CHB-MLI, respectively, raising the inverter footprint and cost Further, in NPC-MLI and FC-MLI, enlarging level count renders extra challenges of balancing the capacitor voltages, increasing switching frequency, sensor count and control complexity, reducing the inverter reliability and lifetime [12]. To address those shortcomings of the conventional MLIs, many MLIs have been intensively introduced with a focus on a high-level count or specific applications. However, only few publications aim to develop four-level MLIs for low- and medium-voltage three-phase systems, which are briefly discussed hereafter and detailed in [20]–[28]. The authors in [20] introduced an eighteen-step inverter (EI) topology, generating four voltage levels by using twelve switches, twenty-four diodes, three DC-link capacitors, and one DC source. As compared to most four-level topologies, the EI topology requires fewer active switches and does not need any flying capacitor. However, it suffers from using a high count of clamping diodes and high-voltage rating of the semiconductor devices (e.g. when applying a DC-link voltage of 3E, six switches block 3E, six switches block 2E, twelve diodes withstand for 2E and twelve diodes subject to E).

A hybrid π-type topology was reported in [22], eliminating clamping diodes in both EI and NNPC. However, the hybrid π-type requires an addition of twelve switches and three flying capacitors as compared to the EI circuit, or needs six additional switches while saving three flying capacitors as

compared to the NNPC. Despite removing clamping diodes, the hybrid π-type topology still has a high count of switches (twenty-four) besides using three flying capacitors, increasing its cost and size. Alternatively, a four-level active neutral-point clamped (4L-ANPC) topology was reported in [23] to eliminate flying capacitors in the hybrid π-type inverter while using the same switch count. It consists of twenty-four switches, three DC-link capacitors, and single DC source. It is worth mentioning that the switch count can be reduced to eighteen instead of twenty-four by replacing twelve switches with only six switches at the double voltage rating. The authors in [24]–[26] presented a nested T-type (NT-type) MLI, consisting of six switches and two flying capacitors per each inverter leg. The three inverter legs share the same DC-link, which is formed by a single DC source without using DC-link capacitors. Similarly, the π-type inverter in [28] uses the same counts of switches, DC sources, and DC-link capacitors. Both two circuits can eliminate flying capacitors and clamping diodes, being considered as their main merits. However, they still suffer from a high-voltage stress of the full DC-link voltage applied on six switches out of eighteen switches, restricting the reachable output voltage and increasing the switching losses. To tackle the limitations of the aforementioned MLI topologies, namely high counts of flying capacitors, diodes, switches, and DC sources, this paper proposes a novel three-phase four-level topology with a reduced component count to mitigate those problems in low and medium voltage systems. The proposed topology does not need any clamping diode or flying capacitor and uses only eighteen switches for producing same 4-level voltages, resulting in a compact design, and increasing efficiency and lifetime.

II. LITERATURE SURVEY

1. ‘‘Analysis and control of a hybrid-clamped four-level type converter

This paper introduces a hybrid-clamped four-level π-type converter for low-voltage (e.g. 380V) motor drive and other applications. It is based on a four-level π-type converter, with two additional switching devices as well as one flying capacitor (FC) to address the dc-link neutral point balancing issue. This converter has more redundant switching states to be selected in each phase-leg, and consequently, can operate under high modulation indices and high power factors with balanced dc-link capacitors voltages. The switching states with their associated output voltage levels have been analyzed. A carrier-based modulation method with an optimized switching state selection has been devised to modulate the converter and regulate the dc-link neutral points' voltages and the FC voltage. The voltages of the three dc-link capacitors and the FCs can be well controlled with a single-ended configuration (inverter or rectifier). Simulation and experimental results have validated the topology, modulation and control strategy.

2. Topology and control of a four-level ANPC inverter,

Four-level hybrid-clamped inverter is a newly proposed topology that can operate under a wide voltage range without switches connected in series. However, when it is applied in medium voltage high power conversions, the flying capacitors in each phase will occupy a huge volume and a high switching frequency is required to restrain the voltage ripples. In order to overcome this drawback, a four-level active neutral-point clamped inverter is discussed in this paper, which consists of only six switches and no diodes or flying capacitors are required. In order to balance the neutral-point voltages under the full power factor and modulation index range, a capacitor voltage balance method based on carrier-overlapped pulse width modulation is proposed in this paper. The upper and lower dc-link capacitor voltages are balanced by zero-sequence voltage injection and the central dc-link capacitor voltage is balanced by adjusting the duty cycles of switching signals slightly. Simulation and experimental results are presented to confirm the validity of this method.

3. A sinusoidal pulse width modulation (SPWM) technique for capacitor voltage balancing of a nested T-type four level inverter,

In this letter, a new control method based on the sinusoidal pulse width modulation scheme is proposed to control capacitor voltages of a T-type four-level nested neutral-point-clamped (NNPC) inverter. The

T-type four-level NNPC inverter has a lower number of switches and components compared with other four-level classic and advanced inverters, which make this topology attractive for high-power medium-voltage applications. This topology has been proposed and studied with the assumption of constant dc sources instead of flying capacitors. In this letter, a simple single-phase modulator is developed to balance flying capacitor voltages. The performance and the feasibility of the proposed control technique are evaluated experimentally under a steady-state and transient conditions and for different modulation indexes and loads. The experimental results demonstrate the effectiveness of the developed control method to control the capacitors' voltages.

4. ‘‘A new four-level converter for low and medium voltage applications,’’

The paper presents a new four-level voltage source converter (VSC). Compared to conventional four-level converters, this proposed converter has fewer components and can be used for a higher power density system in low and medium voltage applications. Its principles and advantages are studied in this paper. The effect of various redundant switching states on the voltages of flying capacitors is analyzed. The voltages of flying capacitors can be balanced by selecting proper redundant switching states. A carrier-based pulse width modulation (CBPWM) is used to control the proposed converter. The performance of the converter is investigated and simulated in MATLAB/Simulink as well as on a 5 kVA experimental prototype.

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5. ‘‘A capacitor voltage-balancing method for nested neutral point clamped (NNPC) inverter,’’

A capacitor voltage-balancing method for a nested neutral point clamped (NNPC) inverter is proposed in this paper. The NNPC inverter is a newly developed four-level voltage-source inverter for medium-voltage applications with properties such as operating over a wide range of voltages (2.4–7.2 kV) without the need for connecting power semiconductor in series and high-quality output voltage. The NNPC topology has two flying capacitors in each leg. In order to ensure that the inverter can operate normally and all switching devices share identical voltage stress, the voltage across each capacitor should be controlled and maintained at one-third of dc bus voltage. The proposed capacitor voltage-balancing method takes advantage of redundancy in phase switching states to control and balance flying capacitor voltages. Simple and effective logic tables are developed for the balancing control. The proposed method is easy to implement and needs very few computations. Moreover, the method is suitable for and easy to integrate with different pulse width modulation schemes. The effectiveness and feasibility of the proposed method is verified by simulation and experiment.

III. PROPOSED TOPOLOGY

Fig. 1 shows the proposed topology, consisting of twelve unidirectional switches (S1-S12) and three bidirectional switches (B1-B3). It does not use any power diode or flying capacitor, reducing control algorithms complexity, power loss and increasing the inverter lifetime. To simplify the gate-drive circuits, the common-emitter structure is adopted to configure the bidirectional switches. Further, the three-phase legs share the same DC-link, reducing the counts of DC sources and DC-link capacitors. Depending on the availability of the DC sources or applications, the DC-link of the proposed topology can be configured in two ways: either using three low-voltage DC sources or single medium-voltage DC source linked to three DC-link capacitors as shown in Figs. 1(a) and (b), respectively. Renewable

energy systems based on PVs and fuel cells (FCs) have multiple DC sources, thus the first configuration is recommended to be used in those energy systems.

Accordingly, DC-link capacitors and their associated control algorithms can be eliminated. However, power electronic conditioner circuits are needed to control/maximize the raw generated power from those renewable energy sources. On the other hand, the second configuration or single source configuration (SSC) in Fig. 1(b) is recommended for industrial applications, where a single medium-voltage bus is available. Both configurations are detailed in this paper.

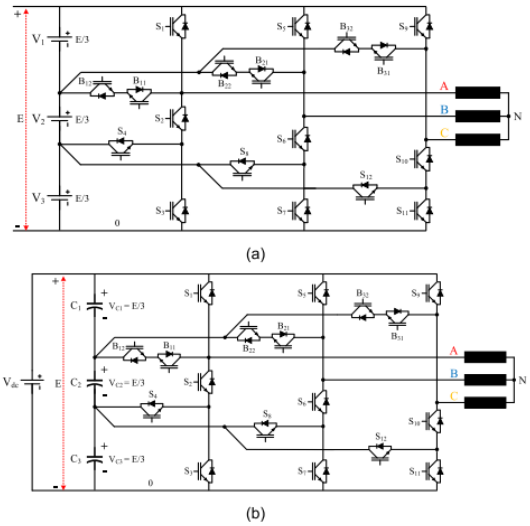


Fig 1: The proposed four-level topology. (a) Multiple sources configuration (MSC), recommended for energy systems, (b) Single source configuration (SSC).

The inverter switches are controlled to produce four unipolar voltage levels of 0, E/3, 2E/3, and E in the pole voltages VA0, VB0, and VC0. Seven-level bipolar voltages can be generated in the line voltages VAB, VBC, and VCA by subtracting the adjacent pole voltages. For example, VAB is synthesized by subtracting VA0 from VB0, producing a seven-level voltage of −E, −2E/3, −E/3, 0, E/3, 2E/3, and E. The operating modes of the proposed topology are illustrated in Fig. 2, showing the switching states for producing seven voltage levels in the line voltage VAB. Each state is accompanied by its corresponding paths for the positive and negative currents. For example in Fig. 2(a), the state I shows that the switches S1, S6, and S7 must be in ON-state to obtain the maximum positive voltage of E in the line voltage VAB while switches (S2-S4), (S5, S8) and (B1, B2) are in OFF-state. The positive and negative currents are highlighted in blue and red dash lines, respectively. Similarly, switching states from II to VIII in Fig. 2 explain the different switching modes of the proposed topology for producing the remaining voltage levels. It should be noted that some switching states are removed when forming these switching paths, preventing the short-circuit faults in the inverter. For example, in leg A, the switching combinations of (S1, S2, S4), (S1, S2, S3), (S3, S4), (S1, B1), and (B1, S2, S4) are marked as unused states in both switching algorithms.

A. MODULATION STRATEGIES

Two modulation strategies are utilized in this section to control the output voltage of the proposed topology. The low-frequency modulation (LFM) is adopted for reducing the switching loss, while the level-shifted pulse width modulation (LSPWM) is implemented for increasing the controllability of the output voltage. Both switching strategies follow the provided switching states in Table 1 to create the switching pulses for the proposed inverter. Table 1 shows the switching pattern of switches (S1-S4) and B1 for producing four levels in the pole voltage VA0. Both sinusoidal and modulator signals can be varied in their magnitude from 0 to 1, providing two degrees of freedom for producing voltages at different RMS, level counts, and THDs. For example, selecting a magnitude value of 1 for the three sinusoidal signals and ±0.35 for H modulators can produce seven-level line voltages with THD of 11.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 12, No. 2, December : 2023

81%. On the other hand, five-level line voltages with the THD of 34.88% are educed when H modulators are equal to ±0.9.

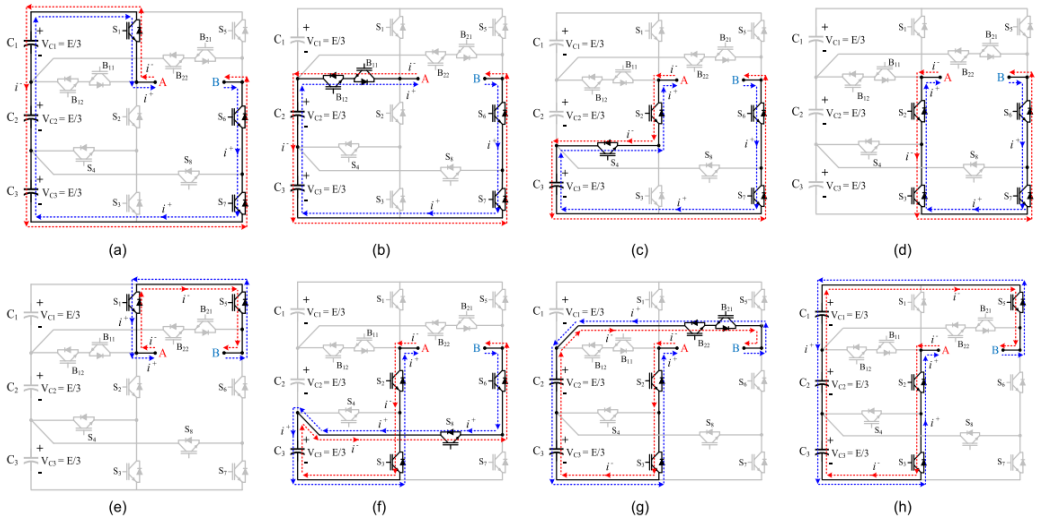


FIGURE 2. Switching states of the proposed topology

VA0 with four voltage levels of 0, E/3, 2E/3, and E, being marked by the switching states in Table 1.

TABLE 1. Switching states for producing four voltage levels in pole voltage VA0 .

State	V_{A0}	S_1	S_2	S_3	S_4	B_1
A	E	ON	OFF	OFF	OFF	OFF
B	$2E/3$	OFF	OFF	OFF	OFF	ON
C	$E/3$	OFF	ON	OFF	ON	OFF
D	0	OFF	ON	ON	OFF	OFF

IV. VOLTAGE BALANCING CONTROL OF THE DC-LINK CAPACITORS

The capacitor voltage imbalance is common in four-level inverter topologies, where three capacitors are connected in series to divide the DC-link voltage into three equal parts as shown in Fig. 1 (b). A generalized mechanism for investigating the capacitor voltage imbalance in the four-level topologies was provided in [27]. The three capacitor currents IC1, IC2, and IC3 in the single source configuration (SSC) of the proposed topology are not equal, causing a voltage
imbalance. Fig. 5 describes the basic principle of the voltage balance control for the proposed topology, consisting of modulation signal generation block, carrier signal block, and the proportional-integral (PI) controller-based voltage loop. These three parts are used to generate modulation signals with a third-harmonic injection, variable and fixed carrier signals, and regulate the C2 voltage at Vdc/3. The three carrier signals, CR1, CR2, and CR3, have the same phase shift and frequency, but are different in the amplitude and level shift. CR1 and CR3 have a fixed amplitude of 1.5, and are shifted in level of 1.5, but the amplitude of CR2 is variable. It can be any value from 0 to 1.5β, where β is the PI output. Increasing the amplitudes of CR1 and CR3 compared to the LSPWM in Fig. 4 raises the duty cycles of S1 and S3 (dS1 and dS3) as shown in Fig. 6, discharging more energy from (C1 and C2) and (C2 and C3), respectively. On the other hand, the duty cycles of B12 and S2 (dB12 and dS2) are changing through the PI controller, aiming to regulate the middle capacitor voltage VC2 at Vdc/3. Accordingly, the capacitor voltages are effectively balanced.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 52, Issue 12, No. 2, December : 2023

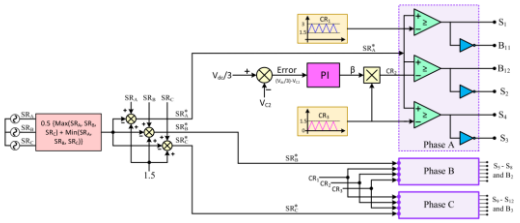


FIGURE 3. Overall voltage-balance control of the DC-link capacitors.

V SIMULATION RESULTS

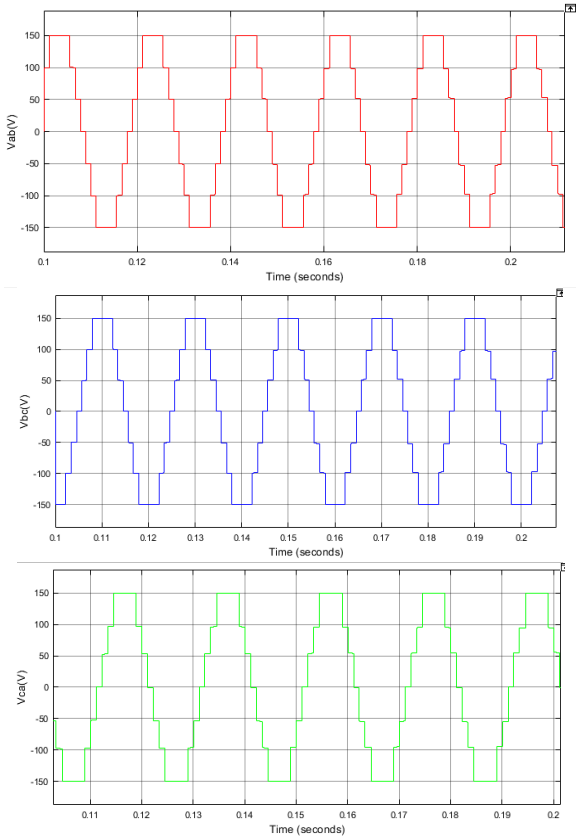
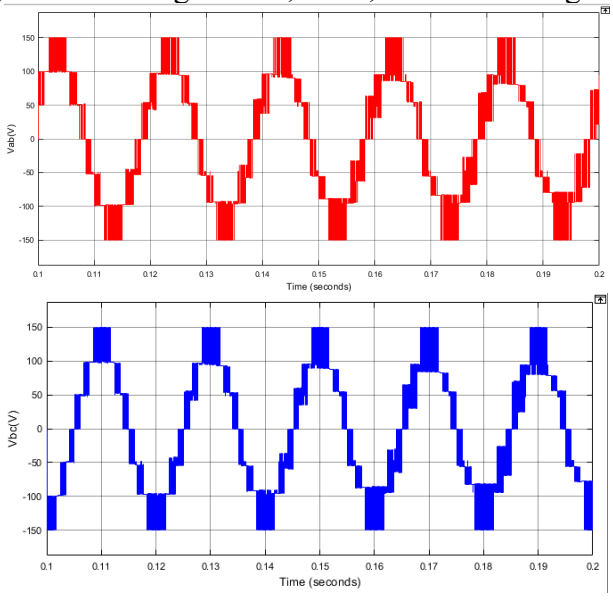


Fig 4: Line voltages VAB, VBC, and VCA using LFM



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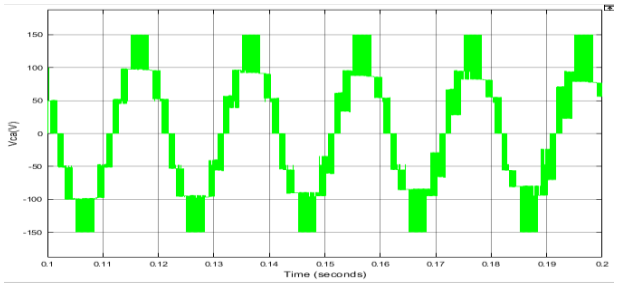


Fig 5:Line voltages VAB, VBC, and VCA using LSPWM

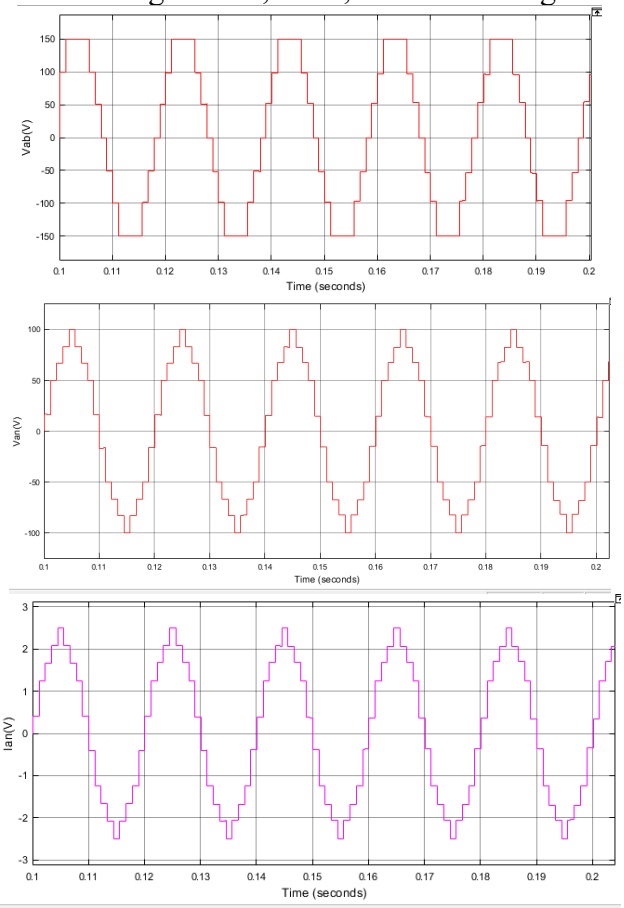
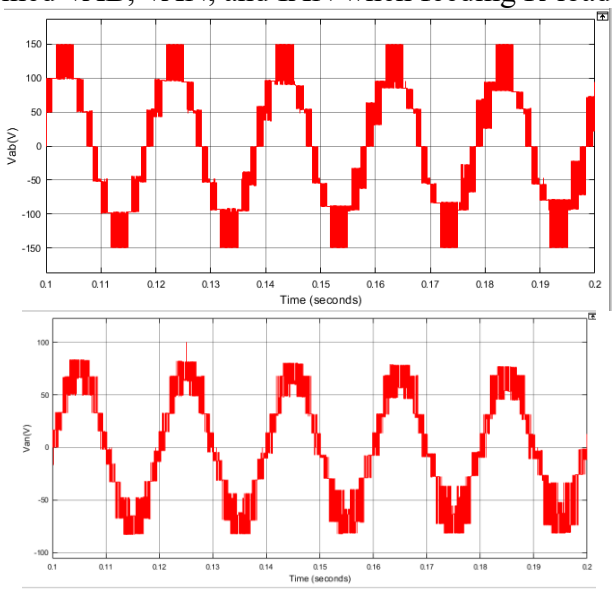


Fig 6:. Obtained VAB, VAN, and IAN when feeding R-load using LFM



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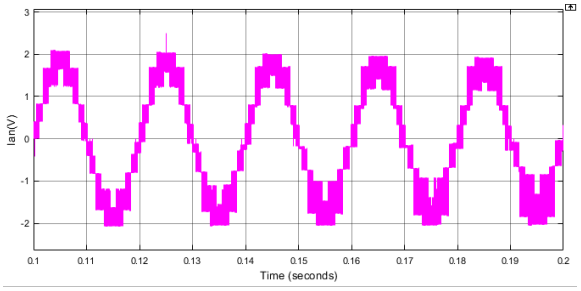


Fig 7:Obtained VAB, VAN, and IAN when feeding R-load using LSPWM

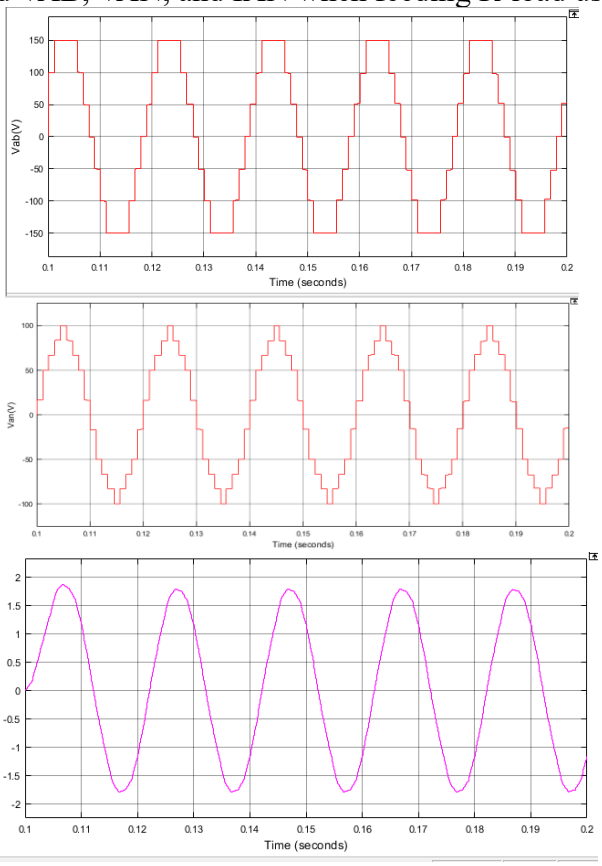
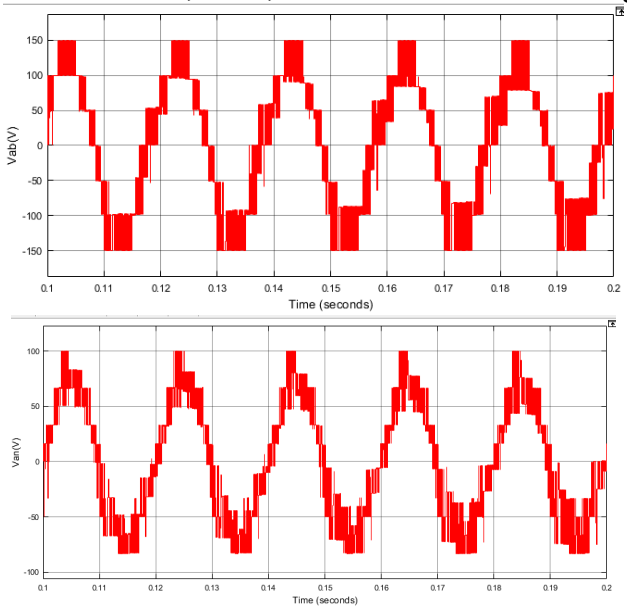


Fig 8. Obtained VAB, VAN, and IAN for R-L load using LFM



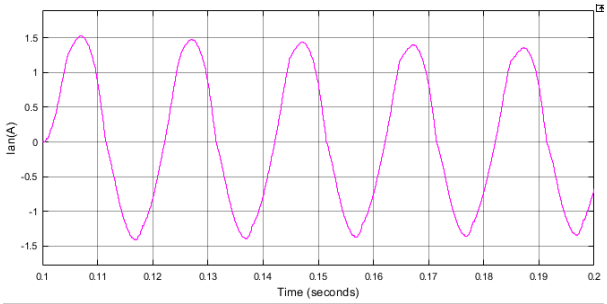


Fig 9:Obtained VAB, VAN, and IAN for R-L load using LSPWM (a) Simulation,

VI: CONCLUSION

This paper proposes a novel inverter topology with a reduced component count, being attractive in low- and medium-voltage applications. The proposed circuit generates four voltage levels without requiring flying capacitors or clamping diodes, reducing the size, cost, control complexity of the inverter and enhancing its reliability and lifetime. Several simulation and experimental tests were presented to validate the proposed topology performance at resistive and inductive loads. The proposed inverter was compared with the recently developed four-level topologies to highlight its merits. Moreover, its conversion efficiency was analyzed when varying the switching frequency, modulation schemes, and loads.

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