Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 8, No.1, August : 2024

DESIGN AND IMPLEMENTATION OF AREA & ENERGY EFFICIENT MODIFIED SRAM CELL USING QUANTUM CELLULAR AUTOMATA

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ABSTRACT
The rise in popularity of memory devices can be attributed to the increasing use of advanced portable electronic devices. Among the various memory systems, Static Random Access Memory (SRAM) stands out due to its high speed and low Energy consumption. The conventional 6T SRAM design using Complementary Metal-Oxide-Semiconductor (CMOS) technology has limitations in terms of scalability and Energy consumption. Quantum-dot Cellular Automata (QCA) is a promising alternative technology that offers advantages such as Lower Latency, lower Energy consumption. In this research paper an SRAM_QCA_26 cell design has been proposed which involves the use of a 6T SRAM cell architecture implementation using controlled buffers and inverter loop. The performance metrics of the SRAM_QCA_26 cell design is analysed using QCA Designer Tool 2.0.3. The simulation results show that the SRAM_QCA_26 cell design offers higher speed and lower Energy consumption compared to the conventional CMOS-based 6T SRAM design and QCA based SRAM implementations. The SRAM_QCA_26 cell design also exhibits better reliability due to the immunity of QCA technology to some of the problems faced by CMOS technology, such as the leakage current and thermal noise.TheSRAM_QCA_26 cell design shows lower latency of 0.75 clock cycles, area of 0.06 μm^2 and energy dissipation of 7.65e-003 when simulated using QCA Designer Tool 2.0.3 and QCA Designer-E,the simulation results are better in terms of area, Energy and Latency when compared to existing 6T CMOS SRAM and QCA based SRAM designs. The SRAM_QCA_26 cell design is testable as the design follows symmetrical Architecture from input side to output.

Keywords: SRAM Cell, low Area, Latency, design for testability, QCA, Low Energy dissipation, QCA Designer.

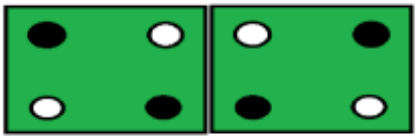
Introduction
As feature sizes in CMOS continue to decrease, limitations persist [1], driving rapid developments in nanoscale molecular designs. QCA finds a compelling application in Static Random Access Memory (SRAM) due to its homogeneous structure, ideal for nanoscale fabrication. Noteworthy architectural innovations include parallel memories, optimizing memory cell design for efficient data movement Quantum-Dot Cellular Automata (QCA) [2] represents a ground breaking technology utilizing quantum dots for digital computation. This innovative approach brings forth substantial improvements, including decreased Energy consumption, minimized delay and speed in data transmission. QCA is best suitable to implement reversible designs [3,4,5]. Unlike conventional technologies such as CMOS, QCA operates without a voltage source, where electron positions dictate logical values. Moreover, QCA introduces a novel paradigm shift in clocking mechanisms, with the clock altering the barriers between dots to regulate electron tunnelling. High operational speed/frequency (in the range of THz), high device density, and low Energy dissipation is possible with QCA Technology. In order to address the problems with CMOS, QCA is drawing researchers to develop a variety of digital circuits in QCA Technology [6], including flip flops, shift registers, adders, multipliers, multiplexers, encoders, decoders, and content addressed memory. The proposed SRAM_QCA_26 cell design demonstrates superior performance in terms of area and delay compared to CMOS-based counterparts [7] and QCA based SRAM designs [8].
A memory cell is the basic unit of a memory array. Static Random Access Memory (SRAM) is the fundamental and most vital memory technology. It is fast and robust and finds its application in the design of many digital circuits [9] including microprocessors and microcontrollers. The scaling of

transistors has increased the demand for larger and faster microprocessors and the demand for high-density and high-speed SRAM. Hence, there is a need to design efficient SRAMs for low-Energy and ultra-dense applications. In this paper, an optimized design of SRAM is presented using QCA Technology, Energy consumption, area and latency calculations have also been performed for molecular QCA implementation of the same design.

2. Basics of QCA Technology

QCA is emerging as a prominent nanotechnology, offering high switching speeds, low Energy consumption, and reduced area requirements. Its computational principles rely on electrostatic interactions among QCA cells. The fundamental unit of QCA computation is typically a four-dot cell. In **Figure 1**, an unoccupied dot is denoted by a white circle, while an occupied dot is represented by a black circle. Electrons within QCA cells tend to occupy diagonally opposite positions due to electrostatic interactions, creating two distinct charge distributions or logical states. These states are observable and can be leveraged to toggle between logical levels '1' and '0' for a specific bit.

When building digital circuits, QCA substitutes metal islands or quantum dots for transistors. A QCA cell has four quantum dots in it. This is among the essential parts of circuits for QCAs. These 18 nm x 18 nm quantum dots are found at the corners of the cell. In the quantum dots diagonal to each other, there are two free electrons. It is not possible for these electrons to move between the cells, but they can tunnel between the dots. The electrons can be seen as having two polarization states. The values can be either ‘0’ or ‘1’. The cells display these polarization states and information travels between them as a result of the Columbic repulsion between them. The basic QCA cell and its polarization states are depicted in **Figure 1**, the cells connected together to pass data will form a wire [10].



P=+1 (Binary 1) P=-1 (Binary 0)

Fig. 1: Representation of QCA Cell

Four clock levels in a QCA cell guarantee that the signal Energy is dispersed appropriately. These are Switch, Hold, Release, and Relax. This QCA clocking [11] is depicted in **Figure 2**. During the switch phase, the cell switches polarity when the barrier between dots increases, and it maintains its polarity after reaching the barrier during the hold phase. When the cell releases its polarity, it loses its orientation. When the cell reaches the relaxation phase, electrons are free to transfer within. An identical clock signal is sent to the cells within a zone and a sub-array is formed. A maximum of 100 MHz frequency is attainable theoretically in magnetic QCA, up to 1 GHz in semiconductor and 1THz in molecular QCA [12].

A QCA wire and the states of the cells in different clock zones are represented as clock-1, clock-2, clock-3, and clock-4 respectively. These stages are labelled as switch, hold, release, and relax. During the switch period, the barrier potentials are low and the cells remain unpolarized. As the switch stage progresses, the QCA cells become polarized and the potential barriers increase, facilitating computation. Following the hold stage, the potential barriers remain high. During the release stage, the QCA cells depolarize as potential barriers decrease. In the relax stage, the QCA cells continue to remain depolarized as the barriers remain low.

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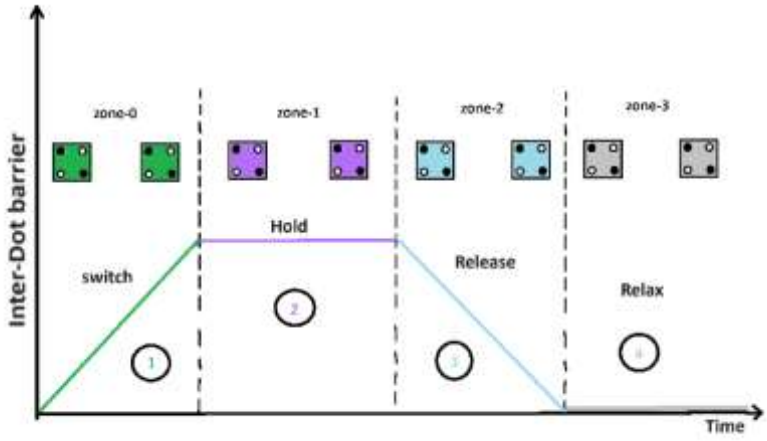

Fig. 2: QCA Cells Polarization of Various Clocking Zones

In QCA logic, a 3-input majority voter (MV) is used to process information, with its output represented as

$$MV (A, B, C) = A.B + B.C + A.C \quad (1)$$

Figure 3 shows how the majority gate functions within QCA, playing a crucial role in logical operations. **Figure 4** demonstrates how a 2-bit AND gate is created using a 3-bit MV. For logical operations like OR and AND, MV (A, B, 1) and MV (A, B, 0) are utilized respectively. Each QCA cell consists of four quantum cells positioned at the edges of a square cell. Within these cells, two electrons can move between adjacent dots, contributing to the computation process.

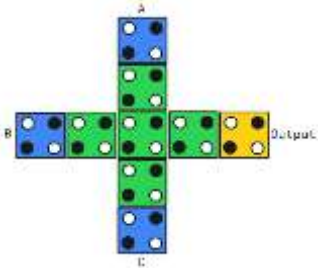

Fig.3: QCA Majority Gate

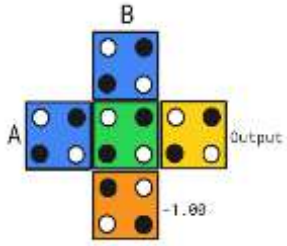

Fig. 4: QCA AND Gate

3. Literature Review

Subhashree Rath and Siba Kumar Panda [13] have proposed the design and implementation of 6T SRAM cells in CMOS process technology, focusing on performance analysis in terms of delay, energy, and static noise margin. They also propose techniques such as low energy supply voltage, memristor-based SRAM, MTCMOS, charge pump circuits, and novel SRAM cell designs to address energy dissipation. Umayia Mushtaq and Vijay Kumar Sharma [14] have designed low-Energy circuits using 6T FinFET SRAM cells at 7nm to address energy dissipation challenges in sub-micrometer regions. Moein Kianpour and Reza Sabbaghi-Nadooshan[15] have proposed a 16-bit × 32-bit SRAM with a new structure in QCA, offering high operating speed due to its pipeline architecture. Saba Rezaie Fam and Nima Jafari Navimipour[16] have designed a loop-based random-access memory (RAM) using nanoscale quantum dot cellular automata (QCA), arguing that QCA offers significant advantages over traditional CMOS technology, such as reduced energy consumption, increased clock frequency, and higher device density. Mostafa Abdollahian Dehkordi et al [17]. have proposed two improved structures for loop-based RAM cells that leverage the inherent capabilities of QCA, aiming to reduce the number of cells, minimize wasted area, and enhance speed compared to traditional loop-based RAM cells. Trailokya Nath Sasamal, Ashutosh Kumar Singh, and Umesh Ghanekar [18] have proposed new architectures for Quantum-dot Cellular Automata (QCA) based D-Flip-Flops and Random Access Memory (RAM) cells using majority gates. These designs demonstrate superior

performance in terms of area and latency compared to previous best designs. The RAM cell occupies an area of 0.12 μm² and has a delay of 1.5 clock cycles. The D-Flip-Flop designs use 14%, 33%, and 21% less area and have 40%, 27%, and 25% less latency for level-triggered, positive/negative edge-triggered, and dual edge-triggered designs, respectively. The D-latch-based nano-scale RAM cell is suitable for efficient single-layer QCA-based circuits, offering low latency and a reduced number of cells. The RAM cell structure with set and reset ability outperforms previous designs in terms of latency, complexity, and area occupation. A new QCA-based RAM cell design using a 3-input rotated majority gate (RMG) [19] is presented for high-speed and low-energy consumption memory. The design uses SR-latch for loop-based RAM cell design, with simulation results showing superiority in delay and cell count.Azath Mubarakali, Jayabrabu Ramakrishnan, Dinesh Mavaluru, Amria Elsir, and Omer Elsier [20] present a D-latch-based nano-scale RAM cell suitable for efficient single-layer QCA-based circuits. The research aims to optimize RAM cell design, reduce latency, and decrease the number of cells. Simulation results show improved efficiency compared to previous designs.Shaahin Angizi, Soheil Sarmadi, Samira Sayedsalehi, and Keivan Navi [21] discuss the design and evaluation of a new majority gate-based RAM cell in quantum-dot cellular automata. They introduce a robust five-input majority gate suitable for efficient QCA circuits in a single layer, with a novel RAM cell architecture with set and reset ability. Sara Hashemi and Keivan Navi [22] introduce new robust QCA D flip-flop and memory structures for QCA technology, showing improved performance compared to previous designs.

The article design and layout of Random Access Memory (RAM) using Quantum-Dot Cellular Automata (QCA) technology[23], is based on a 2D grid of row-addressable memory cells, each utilizing 158 QCA cells. Challenges in QCA design include fault tolerance, clocking delays, and optimization for higher storage densities.Soha Maqbool Bhat, Suhaib Ahmed, Ali Newaz Bahar, Khan A. Wahid, Akira Otsuki, and Pooran Singh [24] propose a cost-efficient single-layer SRAM cell design in QCA technology, which includes 39 cells with a latency of 1.5 clock cycles and improves cell count, area, latency, and cost compared to existing designs.Premananda B.S.[25] discusses the design, implementation, and performance analysis of a compact 4x8 bit SRAM array using QCA technology, addressing energy consumption and area efficiency issues in memory systems, particularly in portable and wireless devices.

4. Implementation of SRAM_QCA_26 cell design using QCA Technology

The two types of approach for designing of memory cells are Line based and Loop based. Line-based [26] approach needs a clock for QCA wire so that data needs to propagate back and forth and it needs additional clock Zone in order to facilitate flow of data through a QCA wire, and storing of data needs additional clock zones making implementation of such memory cell complex. Whereas loop-based memory cell [27] structures use a feedback path loop where data is circulated and stored easily though there is difficulty in employing efficient clocking mechanisms. The loop-based memory cell implementation is more preferred as it doesn't require additional clock zones. The delay of parallel memory cell architecture is less compared to serial memory cell architecture as in parallel only one bit is stored in memory loop, so during read or write operation there is no additional delay wherein in serial access, more bits stored in each memory cell which use shared read or write circuitry, making delay equal to that of word size in memory loop.

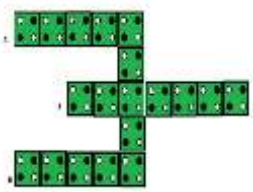

Fig-5 Line-based memory

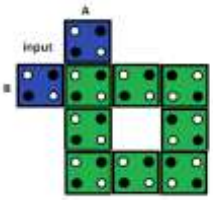

Fig-6 Loop-based Memory

The loop-based memory cell circuitry designing and implementation needs efficient layout mechanisms as memory loop is significantly smaller in size thus raising difficulty and need for using efficient clock zones within that memory loop. The SRAM_QCA_26 cell design implementation is based on Loop based Architecture [28,29,30] in which layout is designed to occupy a smaller number of cells and decrease the latency.

Conventional 6T SRAM Cell consists of 6 transistors form a flip-flop with two cross-coupled inverters as shown in **Figure 7**. SRAM retains information bits in its memory as long as Energy is being supplied, but the data is lost once the Energy supply is disconnected. This research paper presents a low Energy QCA implementation [31] of 6-transistor (6T) CMOS SRAM cell design which consists of loop-based memory cell with controlled buffers as shown in **Figure 8**.

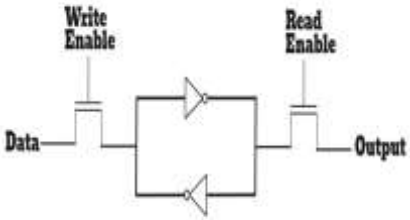

Fig. 7: Representation of 6T SRAM cell

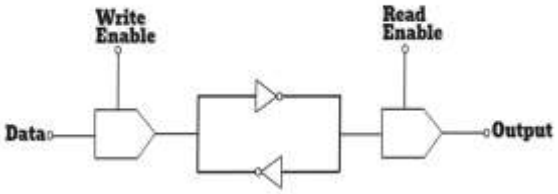

Fig. 8: Representation of 6T SRAM cell with controlled buffer for write & Read

Figure 9(a) & 9(b) represents the controlled buffer and its QCA implementation respectively. In this the data which is given at the input will be transferred to output when control signal is high, otherwise data will not be transferred to the output, the design of controlled buffer needs 9 Quantum cells for implementation.

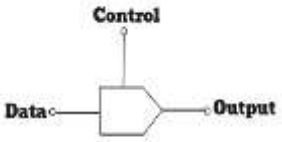

Fig. 9(a): Representation of controlled buffer controlled

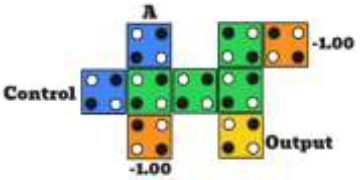

Fig. 9(b): Representation of QCA layout of buffer

The **Figure 10** represents the SRAM_QCA_26 cell design, in which the controlled buffers are used to write the data into the memory loop or to read data from the memory loop .The buffer with Write_enable control designed using clock 0 is used to send the data into memory loop and the buffer with Read_enable control designed using clock 2 is used to read the data from the memory loop.Once the Write_enable is Logic High the input data will enter into the inverter loop designed using clock 1 and the data is stored in the inverter loop, to Read the data stored from the inverter loop the buffer with Read_enable should be High.This SRAM_QCA_26 cell design , which uses the QCA implementation of 6T SRAM cell requires 9 cells for Write_enable buffer,9 cells for Read_enable buffer, 8 cells for the inverter loop and overall the design needs 26 cells and follows the symmetrical Architecture using three clock zones which makes the design Testable [32].

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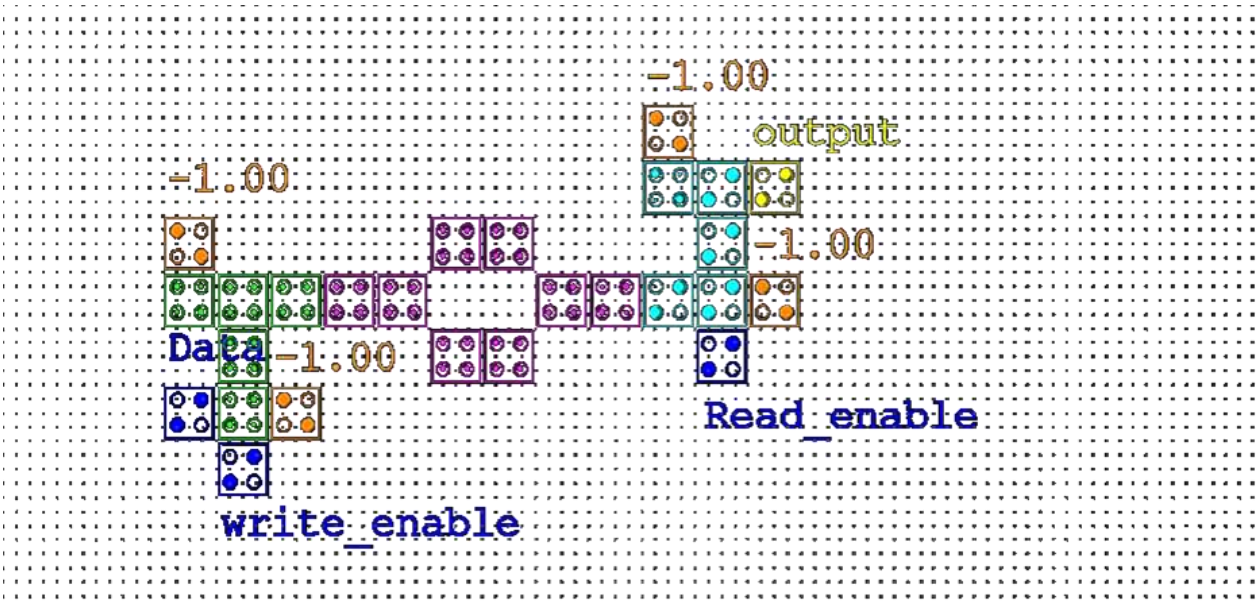

Fig. 10: QCA implementation of SRAM_QCA_26 cell design

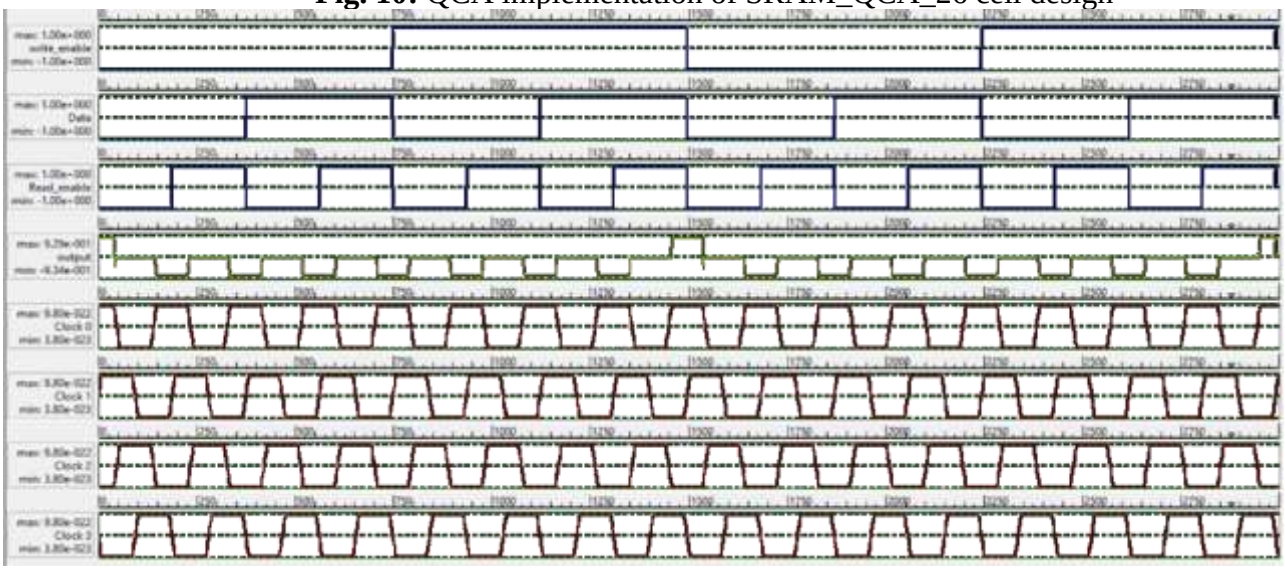

Fig. 11: Simulation results of QCA implementation of SRAM cell

The simulation result of SRAM_QCA_26 cell design is shown in **Figure 11** represents the write and read operations of SRAM memory. SRAM_QCA_26 cell design consists of Read and Write modes. In write mode the data present at the input is written into the memory loop by enabling the Write_enable of input buffer.In Read mode the data stored in the memory loop will be sent to the output once the Read_enable is logic high.The Read ,write modes of SRAM_QCA_26 cell design and the changes in the memory loop for different combinations of Read_enable & write_enable are indicated in Table 1.

Table 1: SRAM_QCA_26 cell design Read and Write Mode operations

Mode	**Write_enable**	**Read_enable**	**Data Write**	**Memory Loop**
Read	0	0	x	No Change
		1		
Write	1	x	0	0
			1	1

5.Simulation Results and Discussions

The simulation results of SRAM_QCA_26 cell design represented in **Figure 11**, exhibits the write and read operations of SRAM memory. Table 2 represents the comparison of Energy Consumption of SRAM_QCA_26 cell design with 6T CMOS, FinFet SRAM Cell at various Technologies, it can be analysed that the SRAM_QCA_26 cell design consumes Energy of 7.65e-0.003 eV which is less compared to previous SRAM design implementations using CMOS at 180nm,90nm,45nm & FinFet 7nm Technologies respectively. Table 3 represents the comparison of Area occupied and Latency of SRAM_QCA_26 cell design with previous SRAM cell designs using QCA which shows that SRAM_QCA_26 cell design occupies less area as it takes only 26 cells of 18nm x18nm for each cell designing SRAM cell and occupies 0.06 $\mu m^2$and has the latency of 0.75 clock phase which is low compared with previous designs of SRAM in QCA Technology.

Table 2: Comparison of 6T CMOS SRAM Vs QCA Implementation of SRAM_QCA_26 cell design

Design	**Technology**	**Energy (eV)**
CMOS 6T SRAM [13]	180 nm	3.24e+12
CMOS 6T SRAM [13]	90 nm	3.7 e+11
CMOS 6T SRAM [13]	45 nm	1.9 e+11
FINFET SRAM CELL[14]	7 nm	8.5 e+10
SRAM_QCA_26 cell design	18x18 nm QCA cell	7.65e-003

Table 3: Comparison of QCA SRAM cell **Vs** QCA Implementation of SRAM_QCA_26 cell design

	Cell Count	**Cell Area (µm2)**	**Total Area (µm2)**	**Latency (Clock Phase)**
[15]	53	0.0168	0.052	1.5
[16]	55	0.0178	0.06	2.5
[17]	63	0.0204	0.092	4
[18]	75	0.0243	0.098	1.5
[19]	87	0.0281	0.12	1.25
[20]	87	0.0281	0.13	1.75
[21]	88	0.0285	0.08	1.5
[22]	109	0.0353	0.13	1.75
[23]	158	0.0511	0.16	2
[24]	39	0.0126	0.046	1.5
SRAM_QCA_26 cell design	26	0.018	0.06	0.75

6. Conclusion

The simulation results of SRAM_QCA_26 cell design exhibits that it occupies less area compared to 6 T SRAM CMOS, FinFets implementations at various Technologies and previous QCA based SRAM designs, as it takes only 26 Quantum cells of 18nm x18nm for each cell and occupies 0.06 μm^2 for the implementation of the design. The total energy dissipated by the SRAM is (Sum_Ebath): 7.65e-003 eV (Error: +/- -2.43e-004 eV), Average energy dissipation per cycle (Avg_Ebath): 6.96e-004 eV (Error: +/- -2.21e-005 eV)SRAM_QCA_26 cell design is energy efficient as it consumes 7.65e-003 eV Energy for the implementation. The energy dissipation of the SRAM_QCA_26 cell design was evaluated using QCA Designer-E. Low-Energy SRAM plays an important role in many types of electronic devices and reduces the overall Energy consumption of the device. The SRAM_QCA_26 cell is designed using a hierarchical approach and implemented in QCA Designer 2.0.3. The SRAM_QCA_26 cell design has latency of 0.75 clock phase. Further The SRAM_QCA_26 cell is

Testable as the design is having symmetrical Architecture from input side to output. The SRAM_QCA_26 cell is designed as a one-bit storage and this can be extended to N x N bit array in future.

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