IMPLEMENTATION OF 16 BIT SFRG TEST PATTERNS FOR DETECTING FAULTS

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Abstract

To provide functional safety, automotive electronics require test solutions, which may be costly. In this study, test pattern generation methods for a ring generator and a 16-bit LFSR are proposed. Random resistive faults and linear as well as structural dependencies are usually held responsible for pseudorandom test patterns' inability to provide full test coverage within an appropriate test application time in LFSR-produced tests that integrate the generation of specific test sequences. The seed-flipping approach selects indiscriminately those portions of a PRPG trajectory that offer the greatest gains in test coverage, as was covered in this section.During in-system test applications, it might be possible to optimize area, power, and test duration. By creating test patterns for a 2-bit and 4-bit input, errors are quickly found.The difficulty of finding defects increases with the size of the circuit. A 16 bit PRPG is used in the first technique that is demonstrated.The following method is seed-flipping PRPG, which is used to periodically supplement PRPG stages. The proposed techniques can be implemented in various in-system testing modes. They can also be simply integrated with a test compression environment. Here, the XILINX program is used to observe the area, power, and timing metrics.

Keywords: Linear Feed Back Shift Register (LFSR), Built-in Self Test (BIST), and Logic Built-in Self Test are some index terms (LBIST)

I. Introduction

Complex integrated electronics are widely used in modern and emerging vehicle systems.Advanced driver assistance systems and driverless vehicles use an increasing number of safety-critical components, with high-end versions comprising hundreds of integrated micro controllers. Automotive electronics require test solutions, which could be expensive to build, to achieve functional safety. This paper offers low-cost test pattern generating strategies for a scan-based hybrid logic BIST of automotive ICs in order to meet the challenges provided by high-quality and long-term reliability requirements. Today, test mode operation is not a major focus of research, but low power design has emerged as an urgent and difficult consumption during functional operation. An increase in peak power dissipation could result in an inductance-related voltage decrease. This could then result in some good die failing the test, causing an unwarranted loss of yield. Testing VLSI devices at a high level costs more money as their size and complexity increase. Although the core goal of factory testing will largely remain the same over the coming years to assure reliable and high-quality semiconductor devices, the environment and therefore test methods may go through a major evolution. The design process, semi conductor technology, and characteristics will be some of the major determinants of its evolution. A pseudorandom pattern generator (PRPG) of some form is typically employed in state-of-the-art techniques to create test vectors. So, these patterns need to be altered in some way. The weighted random pattern testing method is one of the most well-known strategies. Here, a weighting logic modifies the LFSR code bits to provide a test with predetermined probability for the occurrence of 0s and 1s.

II. Literature

This paper described an innovative approach to building ring generators and test data cooperators. The main idea behind the suggested method is to apply a set of changes that preserve the transition function of traditional LFSRs while maintaining their structure. It is demonstrated that when these transformations are used in a specific order, the resulting devices have much better structural characteristics and noticeably better overall performance than earlier methods based on LFSRs and CAS. [2] A logical circuit can be tested using pseudo-random bit sequences produced by a Linear Feedback Shift Register (LFSR). This work implements a Test Pattern Generator that, depending on the control signal, can function as both an internal and an external LFSR. This module is implemented in Vivado for several Primitive polynomials ranging in size from 3 bits to 11 bits, and metrics like usage, power, and timing are examined. The major goal of this work is to combine internal and external LFSR using a control signal in a single module to lengthen the Pseudorandom sequences produced by a Test Pattern generator. In order to do this, lower bit LFSR can be used to generate extended test patterns.[3] This study does a delay and power-based qualitative examination of several pattern generator architectures. uniqueness of the work done in the area of BIST architecture for digital circuits, making it simpler to test this circuit while using less power. These architectures can be applied to reversible logic in the future to cut down on power consumption. [4] a system and technique for efficiently coding test patterns for integrated circuits (ICs) with scan designs and built-in linear feedback shift registers (LFSRs) for generating pseudo-random patterns. A novel LFSR logic model is created and implemented into the system during the initialization process in order to generate test data and perform test vector compression. The LFSR logic model is used to specify and compress test vectors during the creation of test data. Each test vector is individually compressed from every other vector. However, the outcome might be displayed all at once and then given to the user or another system to be processed further or implemented in an integrated circuit to be tested. The current idea involves a test vector with 0/1 values. [5] A mixed Logic is used here. The testing of the circuits is suggested in this work using a hybrid Logic Built In Self Test (LBIST) test approach. Stopped-at testing and At-speed testing are used to analyze stuck-at faults and transition faults.According to experimental findings, the developed technique is useful for pinpointing the locations of faults and reducing test time. [6] Deterministic pattern generation will have an option thanks to LBIST. This experiment's major goal is to cut testing time and storage space without sacrificing the greatest amount of test coverage. Out of all the partition trials done, ATPG is the best choice when there is no restriction on the storage area. However, LBIST will be a preferable choice if there are restrictions on the storage space for the patterns during in-field testing. It is impossible to get high coverage using solely LBIST, so a hybrid strategy that runs LBIST a set number of times before topping up with ATPG would be preferable. [7] Large industrial designs can be challenging to eliminate all Xs from, especially when they involve third-party hard IP blocks. It can also be difficult and impractical to anticipate all potential X-sources. We describe an X-tolerant LBIST solution (XLBIST) that makes use of compressor/decompressor structures that already have Xcontrol logic incorporated into the design for scan-compression deterministic patterns.These structures are used by Automatic Test Pattern Generation (ATPG) to produce effective XLBIST patterns.Any number (or density) of Xs can form patterns, with the consequent test coverage trade-off. Results on high-X density industrial designs show reliable XLBIST coverage.

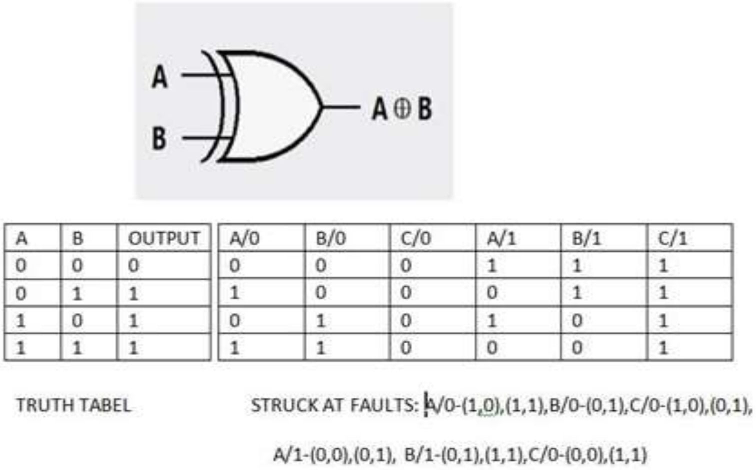
III. Projects Objective Scope

This paper's primary goal is to produce test patterns for the 16-bit LFSR and 16-bit Seed flipping Ring Generator. This leads to the creation of some patterns. Designing a 16-bit LFSR and 16-bit

Seed flipping in ring generator with the appropriate area power and time may be said to be the main goal. This allows for the better observation of area, power, and timing factors.

IV. Testing Vectors

An input stimulus (one signal value for each input signal) and an output response define a test vector (one expected signal value for each output signal).Each test vector is intended to find one or more potential circuit defects.A further way is exhaustive, however employing test vectors to test complex circuits is challenging.then we go for these test patterns.

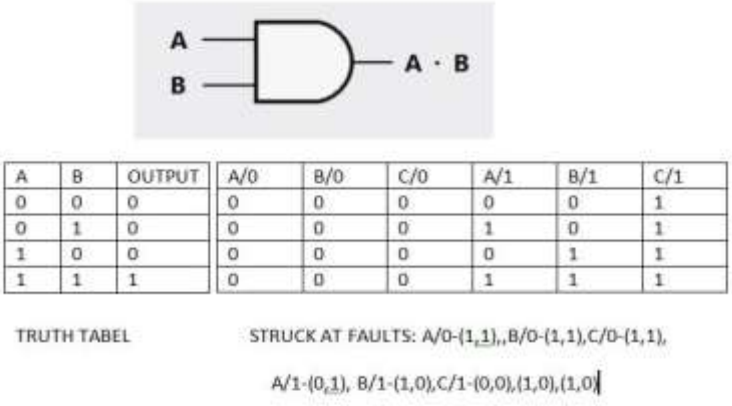


A	B	OUTPUT	A/0	B/0	C/0	A/1	B/1	C/1
0	0	0	0	0	0	1	1	1
0	1	1	1	0	0	0	1	1
1	0	1	0	1	0	1	0	1
1	1	1	1	1	0	0	0	1

TRUTH TABEL

STRUCK AT FAULTS: A/0-(1,0),(1,1),B/0-(0,1),C/0-(1,0),(0,1),
A/1-(0,0),(0,1), B/1-(0,1),(1,1),C/0-(0,0),(1,1)

Figure 1: 2-Input EX-OR Gate



A	B	OUTPUT	A/0	B/0	C/0	A/1	B/1	C/1
0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	1	0	1
1	0	0	0	0	0	0	1	1
1	1	1	0	0	0	1	1	1

TRUTH TABEL

STRUCK AT FAULTS: A/0-(1,1),,B/0-(1,1),C/0-(1,1),
A/1-(0,1), B/1-(1,0),C/1-(0,0),(1,0),(1,0)

Figure 2: 2-Input AND Gate

V. Test Pattern generation

The method of "test compression" is employed to speed up and lower the cost of testing integrated circuits. Using manually crafted test vectors, the first ICs were put to the test. Design for testability (DFT) based on scan and Automatic Test Pattern Generation (ATPG) were created to specifically test each gate and path in a design because it proved to be very difficult to acquire good coverage of probable flaws. These methods had good test coverage and produced very high-quality vectors for production tests. The most straightforward way for developing tests is pseudorandom test creation depends on logic simulation to compute accurate machine results and fault simulation to determine the fault coverage of the test vectors created using a pseudorandom number generator. Types of test pattern generation 1) Deterministic - Developed using ATPG or fault simulation and specific to CUT. Example: Counter address ROM saves test pattern in ROM. 2) Algorithmic – utilised to evaluate particular fault models and regular structures. Consider FSMs. 3) Complete - includes all potential input test patterns. An example would be a circuit with 2n patterns for n inputs. 4) Pseudo-exhaustive: Each sub-circuit that is partitioned is thoroughly tested. Counter, LFSR, and Mux's are examples. 5)Repeatable pseudo-random sequences with characteristics resembling random sequences. 6)Weighted pseudo-random, where some bits generate more 1s or 0s than others. Example: Weighting using LFSR with AND/OR gates. 7) Really random patterns, or randomness True random vector implementation is challenging.

Fault models

STUCK-AT FAULT MODEL: Irrespective of the inputs to the circuit, a signal or gate output is stuck at a 0 or 1 value. BRIDGING FAULT MODEL: When two signals should not be coupled together, they are. This could lead to a wired-OR or wired-AND logic function, depending on the logic equipment used. They are typically limited to signals that are physically adjacent in the design since there are O (n2) probable bridging faults. TRANSISTER FAULTS:CMOS logic gate failures are modeled using the concept of transistor faults. A transistor may be stuck-open or stuck-short at the transistor level. A transistor acts as though it is always conducting current (or stuck-on) when it is stuck-short, and as though it is never conducting current (or stuck-off) when it is stuck-open. A short between VDD will be produced via stuck-short. OPEN FAULT MODEL: In this case, one or more inputs are cut off from the output that should be driving them because it is presumed that a wire is damaged. The ensuing behavior is dependent on the circuit implementation, just like with bridging faults. DELAY FAULT MODEL:The signal finally adopts the right value, although more slowly (or, in exceptional cases, more quickly) than usual in the delay fault model.

IV. Pattern generation using LFSR

Using $X^{16}+X^{15}+X^{13}+X^{4}+1$,this polynomial equation for which we can create random outputs, is developed by 16-bit LFSR. The 16-bit LFSR circuit schematic is displayed in Power reduction is mostly influenced by the technology-specific features of the gates used. A shift register called the LFSR has input that comes via an XOR gate on portion of its input.output is l Flip-flop output is pre-loaded with a seed value, which is anything other than zeros.

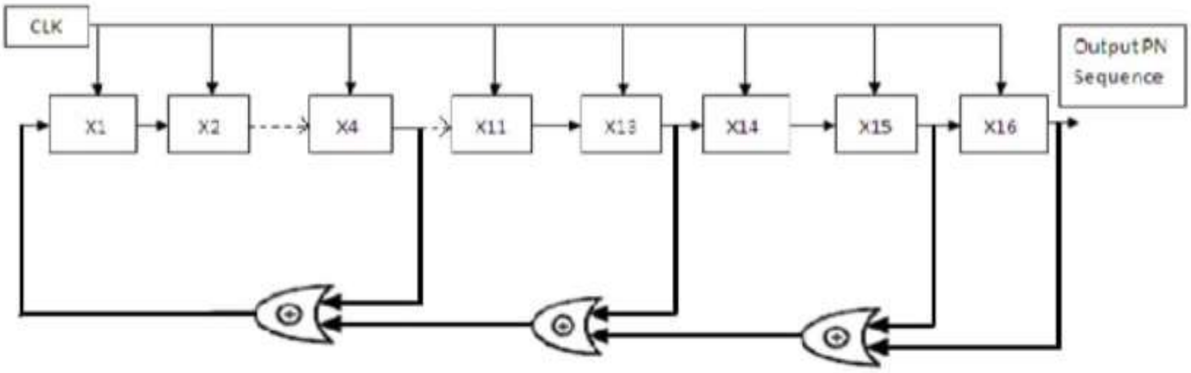


Figure 3: 16 bit LFSR

The polynomial's one's correspond to the input of the first bit. Polynomial term powers are represented by tapped bits, counting from left. The input and output taps are always connected to the first and last bits. The number of taps must be even, and there must be a common divisor among all taps, in order for the maximum length to be attainable. 16-bit LFSR that produces 216 -1=65535 random outputs and has a maximum length feedback polynomial of $X^{16}+X^{15}+X^{13}+X^{4}+1$. Figure depicts a 16-bit LFSR circuit with maximum length feedback that causes all 0 patterns to be produced by the LFSR. When the LFSR is clocked, PRPG produces 0s and 1s.

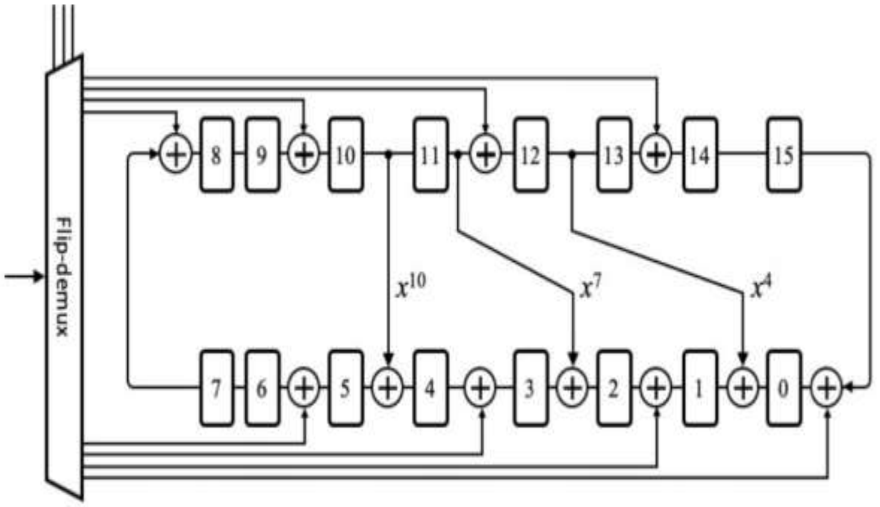


Figure 4: Seed flipping in 16 bit ring generator

Implementing the primitive polynomial equation $X^{16}+X^{15}+X^{13}+X^{4}+1$for 16-bit seed flipping in ring generation. In this case, eight extra XOR gates are positioned so that every other flip-flop inverts its output and provides it to the neighbour to the right. A stage of the ring generator is then inverted if one of the flip-outputs demultiplexer's is asserted. It is important to remember that a somewhat different implementation. A study to confirm each VLSI testing issue has been carried out in order to identify reliable testing procedures that would lower the cost of test equipment.

V. Future scope

(BIST) or built-in test (BIT). BISTs are created by engineers to meet specifications like high reliability and quick maintenance cycles. Other constraints such as: limited technician accessibility and cost of testing during manufacture. BIST's major goal is to simplify systems in order to lower costs and rely less on external (pattern-programmed) test equipment. BIST lowers expenses in two ways: 1. Shortens the test cycle. 2. Decreases the amount of I/O signals that must be driven/examined under tester control, which lessens the complexity of the test/probe setup. A circuit's ability to self-test On the web: 1. Concurrent: running concurrently with regular operations 2. Non-concurrent: inactive throughout routine operations Off line: 1. Diagnostic: practical In S/W or F/W 2. Structural: Based on LFSR The components of a typical BIST design are the Test Pattern Generator (TPG), Test Response Analyzer (TRA), and Control Unit.

GENERATOR OF TEST PATTERNS FOR FAULT DETECTION TEST RESPONSE ANALYZER (TRA): TRA will examine the MISR output and compare it to the LFSR input to determine whether the result is incorrect or not. CIRCUIT UNDER TEST (CUT): The circuit or chip that will be subjected to BIST testing for errors that are stuck at zero or one is the CUT. Safety-critical or high-reliability systems, including engine management, anti-lock braking, passive safety systems, collision avoidance, transmission control, steering control, lane-change assistance, automatic parking, habitat control, in-vehicle infotainment, navigation, and others, frequently incorporate logic built-in self-test (LBIST). However, LBIST must address a number of in-system and in-field testing problems, such as the capacity to conduct periodic tests while carrying out functional operations with extremely fast test application times typically between 5 and 50 ms.

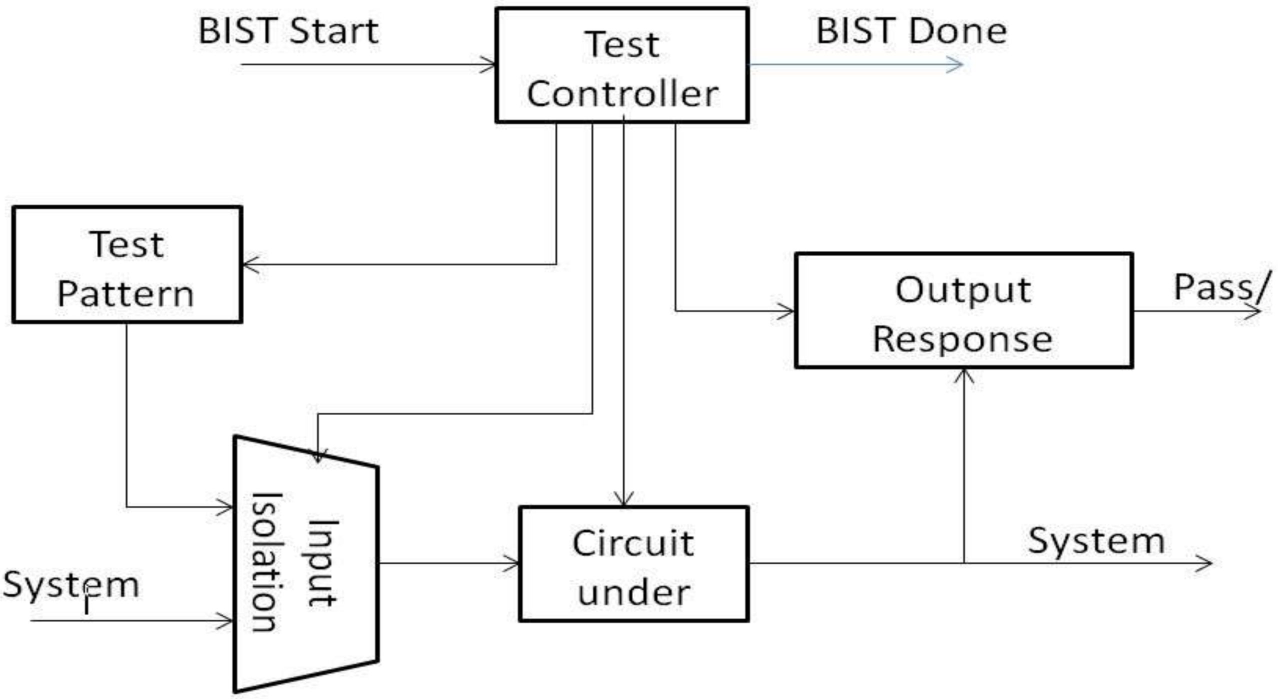
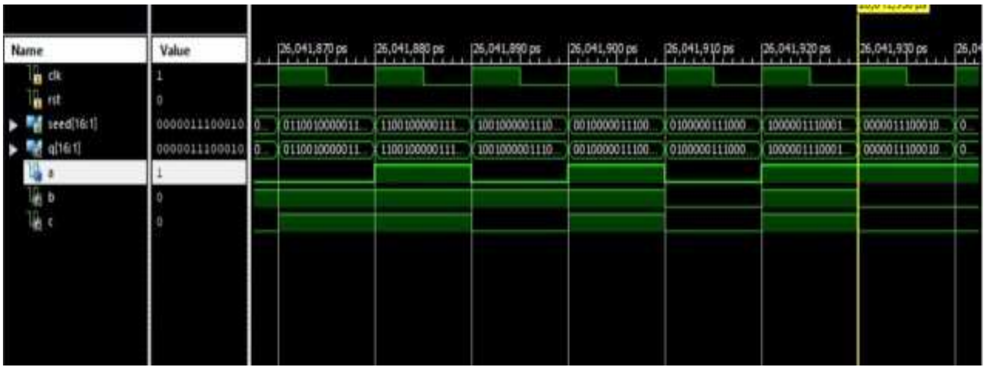
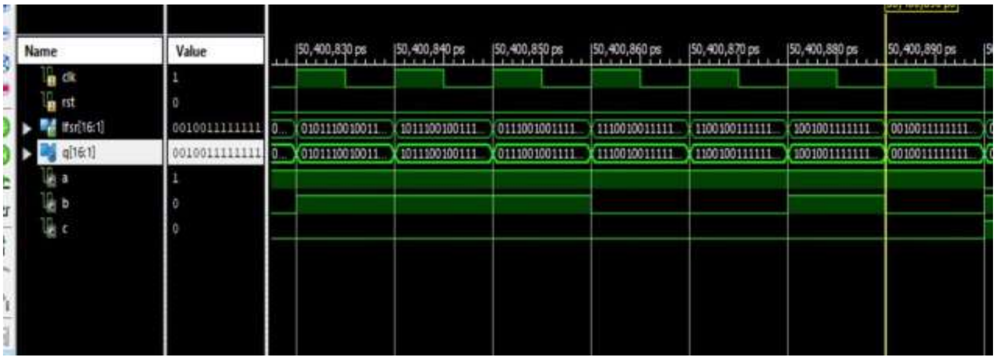


Figure 5:BIST Architecture

Simulation results

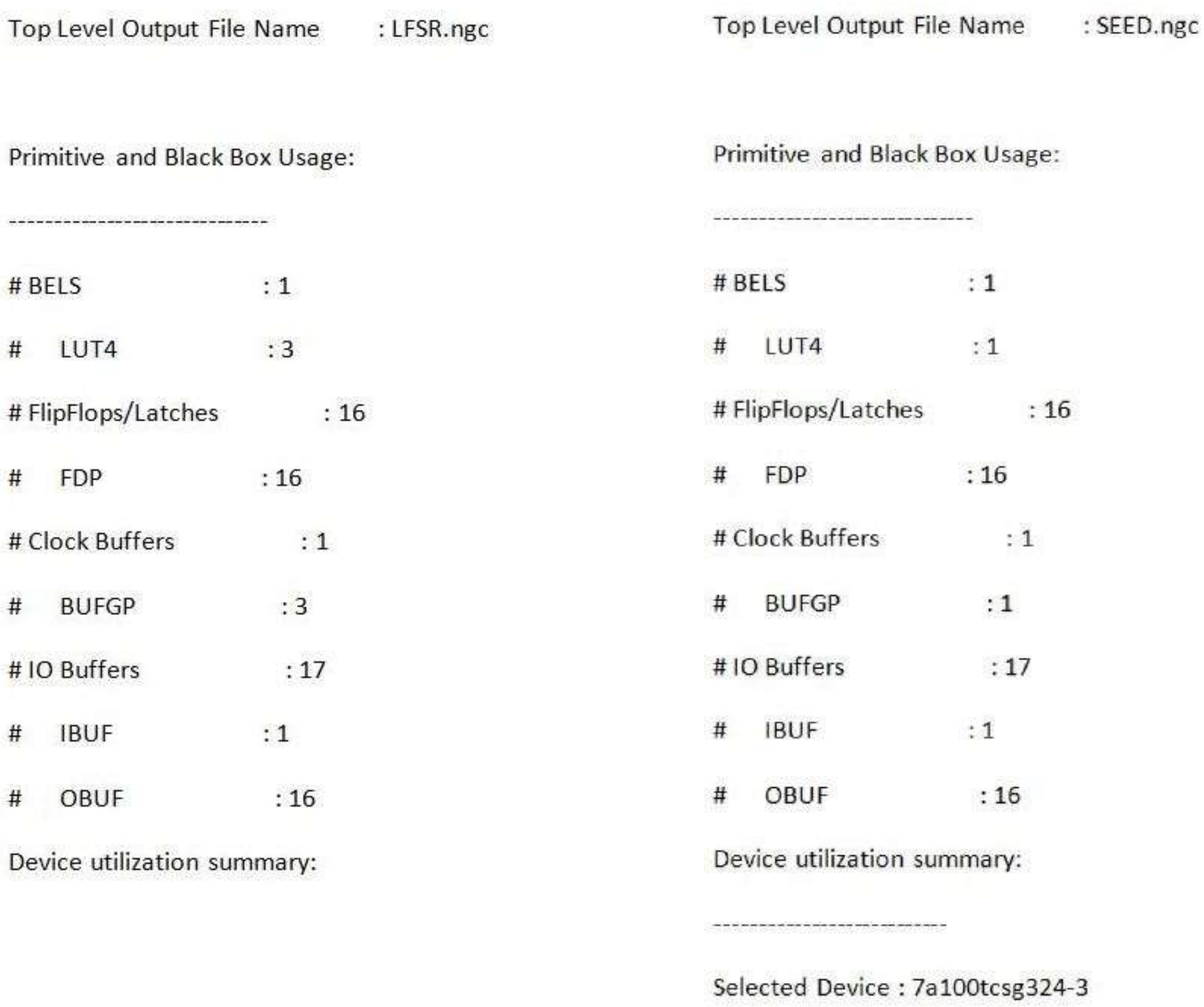


Generation of 16 bit SEED Flipping Ring generator Test patterns



Name	Value
clk	1
rst	0
lfsr[16:1]	0010011111111
q[16:1]	0010011111111
a	1
b	0
c	0

Generation of 16 bit LFSR test patterns



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Top Level Output File Name        : LFSR.ngc


Primitive  and Black Box Usage:

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# BELS                   : 1

#     LUT4               : 3

# FlipFlops/Latches          : 16

#     FDP                : 16

# Clock Buffers             : 1

#     BUFGP              : 3

# IO Buffers              : 17

#     IBUF               : 1

#     OBUF               : 16

Device utilization summary:
```

```
Top Level Output File Name        : SEED.ngc


Primitive  and Black Box Usage:

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# BELS                   : 1

#     LUT4               : 1

# FlipFlops/Latches          : 16

#     FDP                : 16

# Clock Buffers             : 1

#     BUFGP              : 1

# IO Buffers              : 17

#     IBUF               : 1

#     OBUF               : 16

Device utilization summary:

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Selected Device : 7a100tcsg324-3
```

Area report of LFSR and SEED

VLSI I mplementation

PARAMETERS	LFSR	SPEED FLIPPING
TIME	14.00s	11.00s
POWER	1.32W	0.082W

Conclusion

Developing test solutions for automotive electronics is relatively expensive. Problems are rapidly identified by designing test patterns for a 2-bit and 4-bit input. The size of the circuit makes it more challenging to discover flaws. As a result, the test patterns are created by exhaustively and extensively employing the test vectors for the 16-bit SEED FLIPPING LFSR and 16-bit SEED FLIPPING RING GENERATOR. The features of timing, area, and power are computed. Many experimental results indicate that 16-bit LFSR and 16-bit seed ring generator can be employed with on-chip test compression. The 16-bit lfsr is discovered to be superior to the 16-bit seed flipping in ring generator when comparing area, power, and time. When combined with BIST,LBIST,XLBIST.

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