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REVERSIBLE LOGIC GATES AND ITS APPLICATION: A COMPREHENSIVE SURVEY

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Abstract:
The performance requirement increases with the application of computers in domains like artificial intelligence, machine learning, data science, big data, etc. The power consumption increases with an increase in performance. High power consumption, heat dissipation, unable to meet size requirements, and operational speed confines the further development of CMOS technology for circuit designing. Reversible logic is the key to entering into the new era of incredibly compact electronic computational devices with ultra-low power consumption. Reversible logic is an emerging field that is gaining interest as it can overcome the limitations of CMOS technology. It has been proved that any Boolean function can be implemented using reversible gates. This article gives a brief overview of reversible logic gates that have been discovered to date. It also discusses the circuits built using reversible logic gates.

Keywords : Reversible logic gates, reversible computing, power dissipation, garbage outputs, quantum cost, Application of Reversible logic gates, VLSI.

INTRODUCTION:

As predicted by Gordon Moore in 1960,the number of transistors on a chip doubles on average every one and a half years. This is popularly known as 'Moore's Law' [1]. The reduction in feature size has led to several implementation and operational difficulties. It is difficult for CMOS technology to continue with the required level of growth. Since the power consumption of CMOS circuits increases with clock frequency and frequency determines computation speed and performance. An increase in performance also increases power Consumption. The challenge is the unsustainable relationship between power consumption versus performance.

According to Landauer [2][3]the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K=1.3806505*10-23m2kg-2K-1 (joule/Kelvin-1) is the Boltzmann's constant and T is the absolute temperature at which operation is performed Bennett[4] showed that energy dissipation problem is avoided with circuits built using reversible logic gates. In [5] describes the concept of reversible logic which says about the circuit going back at any point for recovering data bit. Hence there is no information that is actually lost and the heat generated during this is also very negligible [6]. Qubit is the term used to describe a single bit of information; 0 or 1; stored in an elementary unit. Any operation on the single bits can be made reversible and hence, quantum circuits and networks.

C. Younis and Knight [7] showed that some reversible circuits can be made asymptotically energy-lossless as their delay is allowed to grow

arbitrarily large. Currently, energy losses due to irreversibility are dwarfed by the overall power dissipation, but this may change if power dissipation improves. In particular, reversibility is important for nanotechnologies where switching devices with gain are difficult to build. The reversibility in computing conveys the idea that

information in the computing state is never lost and is available when needed [8].

Logical reversibility is a process in which the first step can be recovered by back-calculating the result. Physical reversibility refers to no energy dissipation of heat. Logical reversibility is achieved after physical reversibility.[9]The reversible logic gate is a logic device that has n inputs and n outputs. This helps us to distinguish between outputs and inputs, allowing us

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to selectively recover each input from the output. A reversible circuit has 'n' inputs in which 'a' are primary inputs and 'b' are constant inputs
(a+ b = n), and on the output side, there are 'm' primary outputs and 'k' garbage outputs with k + m = n. The reversible circuit is designed with a minimum number of reversible logic gates, a minimum input constant, and a minimum number of garbage outputs.
Currently, reversible logic is used to implement various combinational and sequential circuits like ALU, counters, encoders, flip flops, fault checkers, etc. This article summarizes all the reversible logic gates implemented till date by various authors, explains the working and provides the use case of each reversible logic gate.

BASIC PARAMETERS:

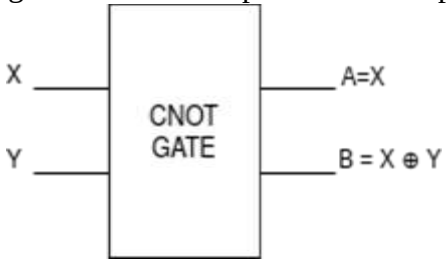
As defined in [5][10] there are several terminologies and parameters related to reversible logics.
Constant inputs: Many Boolean functions are not reversible. Therefore, before realizing these functions, we need to transform them into reversible functions. This conversion is done by a constant input. This is the number of inputs that are held constant at 0 or 1 to synthesize a particular logic function.
Garbage Outputs: Garbage Output is the number of unused outputs in a reversible gate that are unavoidable and are important for achieving reversibility.
Relation:
inputs + constant inputs = outputs + garbage outputs.
Quantum Cost: The quantum cost of a reversible circuit is the total number of 2x2 quantum primitives used to form the equivalent circuit. Some properties of quantum cost are
a.) V*V = NOT
b.) V*V+ = V+ *V = 1 c.) V+*V+ = NOT
Delay: The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. The definition is based on two assumptions: (i)Each gate performs computation in one unit time and (ii) all inputs to the circuit are available before the computation begins.
(Mohammadi & Eshghi, 2009). [A review on reversible logic gates]
Hardware complexity: The hardware complexity determines the number of logical operations performed in the circuit, such as AND, OR, EX-OR.
Flexibility: Flexibility shows the universality of reversible logic gates. To achieve reversibility we need minimal garbage output, minimal delay, and no feedback/loops.

REVERSIBLE LOGIC GATES:

I. 2*2 Reversible logic gates

CNOT/ FEYNMAN GATE:

The input vector is Iv={X,Y} and the output vector is Ov= {X,X $\oplus$ Y}. The first input can pass or invert the second input, hence it is called the controlled NOT gate. The quantum cost is 1. Feynman gate is used for duplication of outputs.[11]



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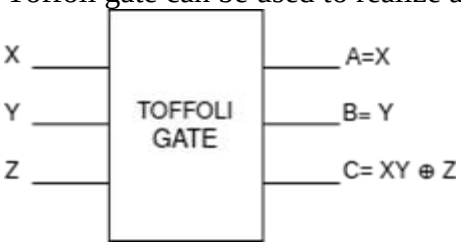
II. 3*3 Reversible logic gates

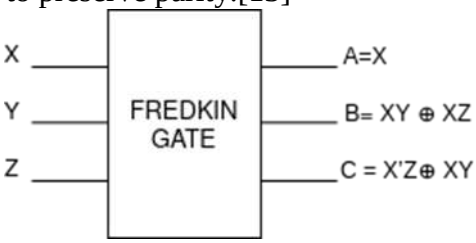
TOFFOLI GATE :

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, Y, XY ⊕ Z}. The last bit is target bit, the rest are control bits, when control bit is 1 the target bit is inverted. The quantum cost is 5. Toffoli gate can be used to realize any function, hence it is known as universal reversible gate.[12]



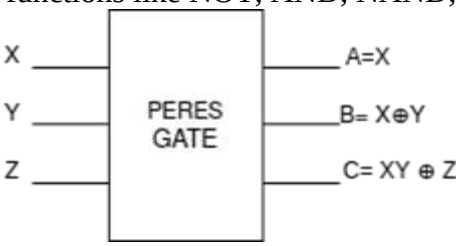
FREDKIN GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, XY ⊕ XZ, X'Z⊕ XY}. The input X is mapped directly to the output A. If X= 0, Y is mapped to B, Z is mapped to C. If X = 1, swap operation is performed and Y is mapped to C and Z is mapped to
B. Therefore it is also known as a Controlled SWAP gate. The quantum cost is 5. Fredkin gate is used to preserve parity.[13]



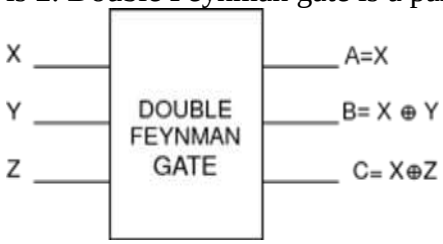
PERES GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, X⊕Y, XY⊕Z}. The quantum cost is 4. TRG gate is used for implementation of a full subtractor. Peres gate can be used to realize functions like NOT, AND, NAND, XOR[12].



DOUBLE FEYNMAN GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, X⊕Y, X⊕Z}. The quantum cost is 2. Double Feynman gate is a parity preserving gate.[14]



BJN GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, Y,(X+Y)⊕Z}. The quantum cost is 5.[15]

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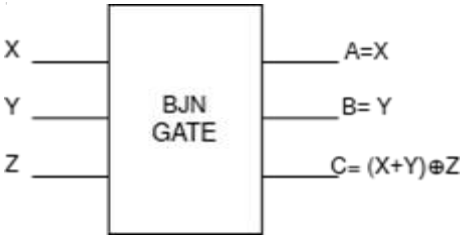
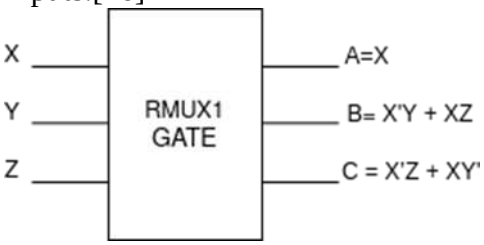


RMUX 1 GATE:

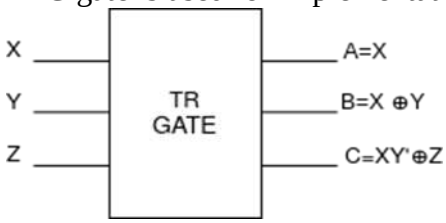
The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, X'Y + XZ, X'Z + XY'}. The quantum cost is 4. RMUX1 works as a 2:1 MUX, where X is the select line and Y&Z are the two inputs.[16]



TRG GATE:

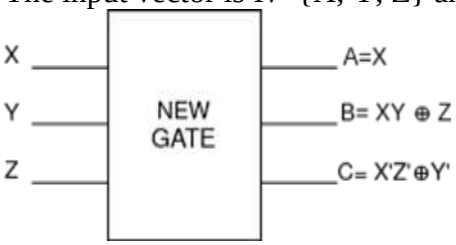
The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, X⊕Y, XY'⊕Z'}. The quantum cost is 4.

TRG gate is used for implementation of a full subtractor.[16]



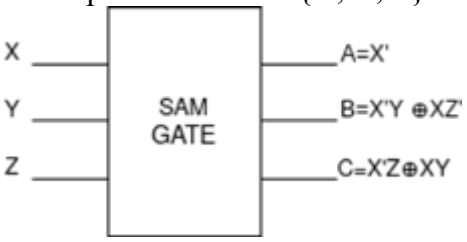
NEW GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, XY⊕Z, X'Z'⊕Y'}.[15]



SAM GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X', X'Y⊕XZ', X'Z⊕ XY}. [15]



NFT GATE

New fault tolerant gate is a parity preserving gate. The input vector is Iv={X, Y, Z} and the output vector is Ov= {X⊕Y, YZ' ⊕XZ', YZ⊕XZ'}. [14]

RC-I GATE:

RC-I gate is a single bit comparator circuit. The input vector is Iv={X, Y, Z} and the output vector is Ov=

{X, X'Y⊕ Z, XY'⊕ Z}. It compares X and Y. [17]

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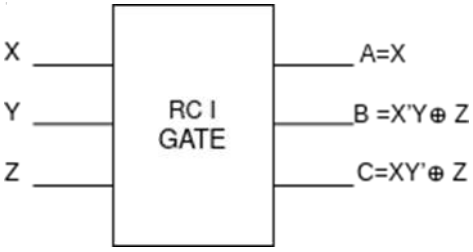
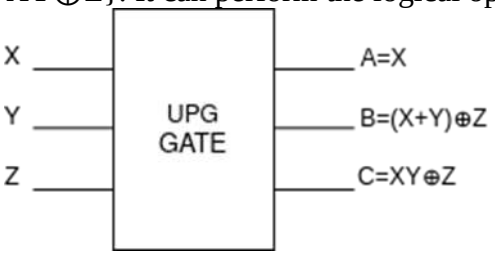


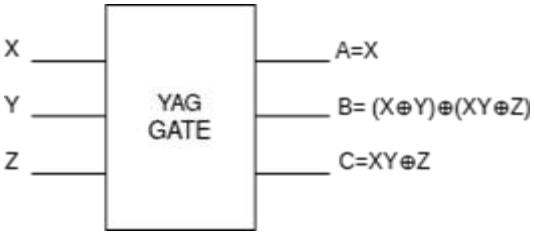
UPG GATE:

Universal Programmable Gate (UPG) can be used to implement logical functions like AND, OR, NAND and NOR. The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, (X+Y) ⊕Z, XY⊕Z}. It can perform the logical operations at low quantum cost.[16]



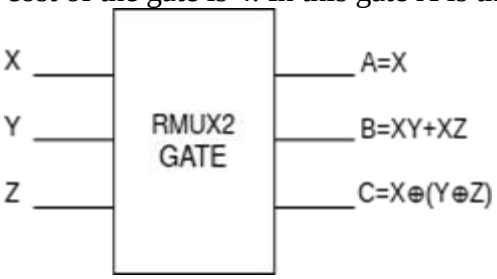
YAG GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, (X⊕Y) ⊕ (XY⊕Z), XY⊕Z}. YAG is used to realize AND and OR functions.[18]



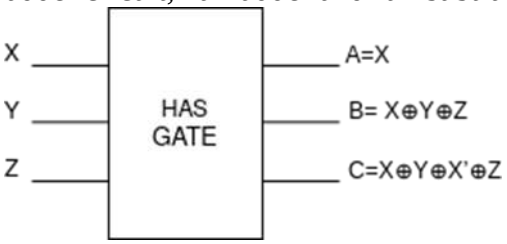
RMUX2 GATE:

The input vector is Iv={X, Y, Z} and the output vector is Ov= {X, XY+XZ, X⊕ (Y⊕Z)}.The quantum cost of the gate is 4. In this gate X is the select line, the gate gives multiplexed output of Y and Z. [16]



HAS GATE :

Half Adder Subtraction gate has quantum cost 5. The input vector is Iv={X,Y,Z} and the output vector is Ov= {X, X⊕Y⊕Z, X⊕Y⊕X'⊕Z}. HAS gate is used to implement BCD adder, carry skip BCD adder circuit, half adder and full subtractor. (Misra et al., 2015). [19]



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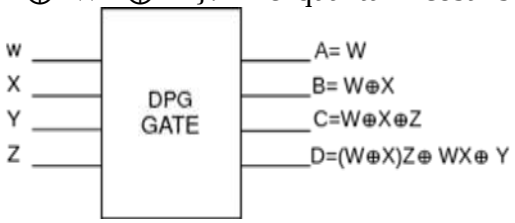
III. 4*4 Reversible logic gates

DOUBLE PERES GATE:

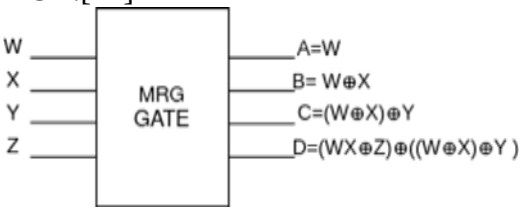
The input vector is Iv= {W, X, Y, Z} and the output vector is Ov= {W, W⊕X, W⊕X⊕Z, (W⊕X) Z⊕ WX⊕ Y}. The quantum cost is 6. Double Peres gate is used to implement full adder.[20



MRG GATE:

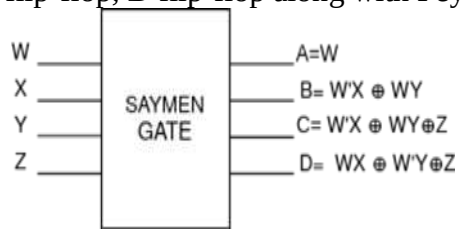
Marrison-Ranganathan gate (MRG) is a programmable gate. The input vector is Iv= {W,X,Y,Z} and the output vector is Ov ={W,W⊕X,(W⊕X)⊕Y,(WX⊕Z)⊕((W⊕X)⊕Y }.

The quantum cost is 6. MRG gate can perform 4 logical operation namely OR, NOR, XNOR and XOR.[21]



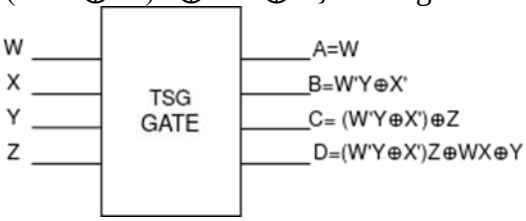
SAYEM GATE:

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W,W'X⊕WY, W'X⊕WY⊕Z, WX⊕W'Y⊕Z}. The Sayem gate can be used to build reversible standard sequential circuits like T flip-flop, D flip-flop along with Feynman gate. [11]



TSG GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W, W'Y⊕X', (W'Y⊕X')⊕Z, (W'Y⊕X')Z⊕WX⊕Y}. TSG gate along with CNOT gate is used to implement full adder .[22]



DKG GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={X , W'Y+WZ', (W⊕X)(Y⊕Z)⊕YZ, X⊕Y⊕Z}. DKG gate can singly work as either a full adder or full subtractor. W is the control line, if W is set to 0 it will work as full adder and if W is set to 1 it will work as full subtractor.[23]

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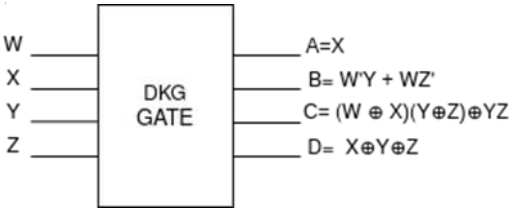
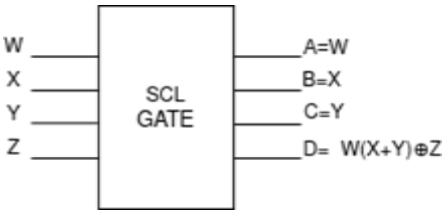


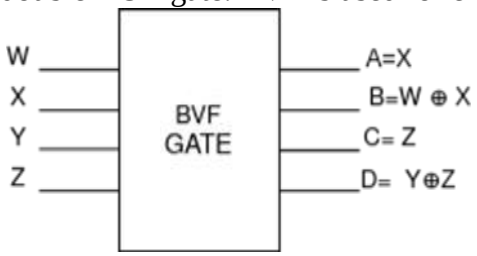
SCL GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W , X, Y, W(X+Y)⊕Z}. SCL gate is used to add 6 to the sum for correcting it to get the actual BCD sum.[20]



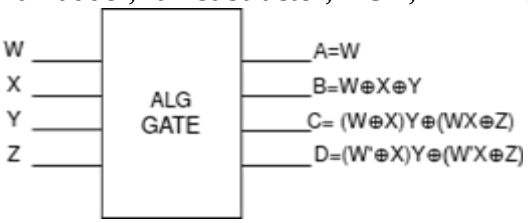
BVF GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W , W⊕X, Y, Y⊕Z}. BVF is a double XOR gate. BVF is used for extracting necessary inputs to meet the fan-out requirements.[24]



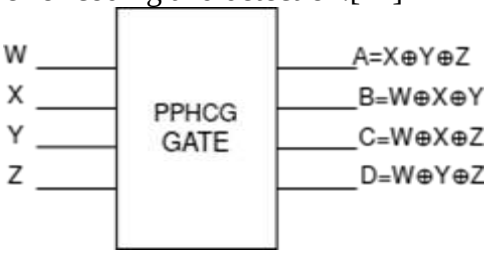
ALG GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W ,W⊕X⊕Y, (W⊕X)Y⊕(WX⊕Z), (W'⊕X)Y⊕(W'X⊕Z) }. The ALG gate can perform multiple operations like full adder, full subtractor, XOR, NAND and NOR. [22]



PPHCG GATE :

Parity Preserving Hamming Code Generating gate is a parity preserving reversible gate. The input vector is Iv={W,X,Y,Z} and the output vector is Ov={X⊕Y⊕Z , W⊕X⊕Y, W⊕X⊕Z, W⊕Y⊕Z}. The quantum cost is 6. PPHCG is used for achieving fault tolerance for the hamming error coding and detection.[14]



IG GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={X , W⊕X, WX⊕ Y, XZ⊕ X'(W⊕Z)} IG gate can be used to perform to perform logical operations like inverter, EX-OR, AND ,EX-NOR and OR. It is a one through gate which means one of the input variable is also the output.[14]

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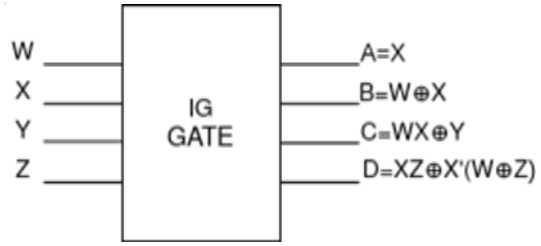
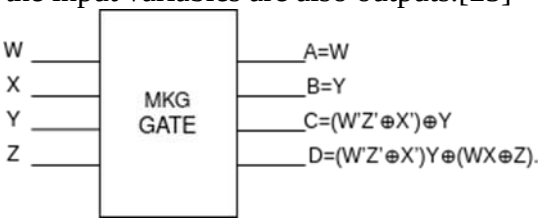


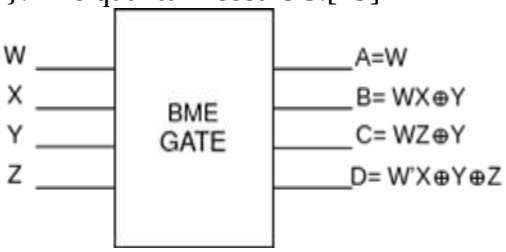
MKG GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W , Y, (W'Z'⊕X')⊕Y, (W'Z'⊕X')Y⊕(WX⊕Z) }. MKG gate is used to realize logical functions like NAND, NOT, NOR ,EX- OR, AND, EX-NOR and OR. The MKG gate is a two- through gate, which means that two of the input variables are also outputs.[25]



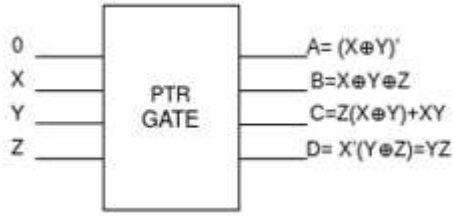
BME GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W , WX⊕Y, WZ⊕Y, W'X⊕Y⊕Z }. The quantum cost is 5.[19]



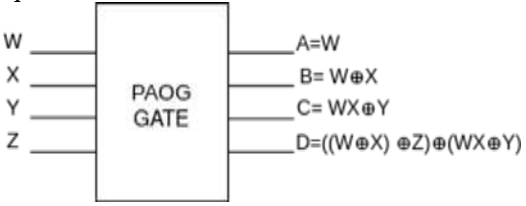
PTR GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={(X⊕Y)' , X⊕Y⊕Z, Z(X⊕Y)+XY, X'(Y⊕Z)=YZ }. [19]



PAOG:

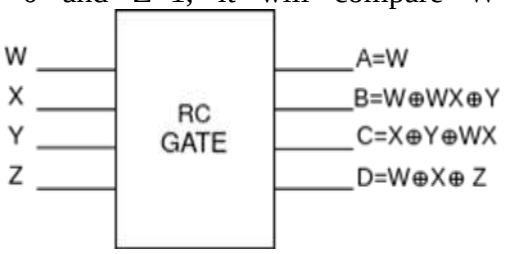
Peres And-Or is an extension of the Peres gate for ALU realization. The input vector is Iv={V,W,X,Y,Z} and the output vector is Ov={W, W⊕X, WX⊕Y, ((W⊕X) ⊕Z)⊕(WX⊕Y)}. When the PAOG is utilized as a programmable reversible logic in gate with two select inputs, it will calculate four logical calculations on those two logical outputs: OR, NOR, AND and NAND.The quantum cost is 6.[16]



RC GATE :

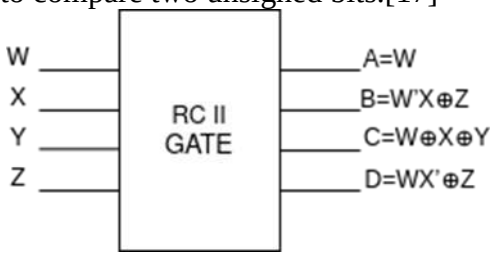
The input vector of Reversible comparator gate is Iv={W,X,Y,Z} and the output vector is Ov={W , W⊕WX⊕Y, X⊕Y⊕WX, W⊕X⊕ Z }.The quantum cost is 5. Y and Z are the control lines when

=0 and Z=1, it will compare W and X.[16]



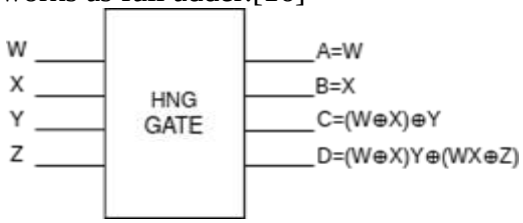
RC-II GATE:

RC-II gate is a reversible sign bit comparator. The input vector of Reversible comparator gate is Iv={W,X,Y,Z} and the output vector is Ov={W , W'X⊕Z, W⊕X⊕Y, WX'⊕Z }. RC-II gate is used to compare two unsigned bits.[17]



HNG GATE :

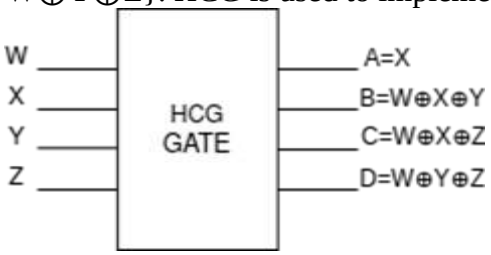
The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W , X, W⊕X⊕Y, (W⊕X)Y⊕(WX⊕Z)}. The quantum cost of the HNG is 6. When Z = 0, the circuit works as full adder.[16]



HCG GATE :

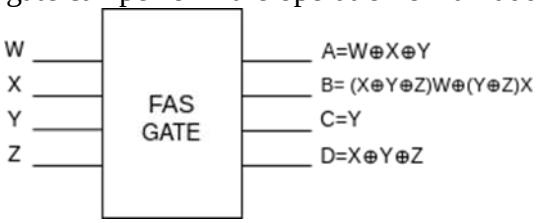
Hamming Code Generating gate (James et al ., 2007) is a one-through gate which means that one of the input variables is also output.

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={X, W⊕X⊕Y, W⊕X⊕Z, W⊕Y⊕Z}. HCG is used to implement Hamming error coding and detection circuits.[19]



FAS GATE :

The input vector is Iv={W,X,Y,Z} and the output vector is Ov={W⊕X⊕Y, (X⊕Y⊕Z)W⊕(Y⊕Z)X, Y, X⊕Y⊕Z}. The gate has a quantum cost of 8. Full Adder Subtraction gate can perform the operation of full adder and full subtraction.[19]



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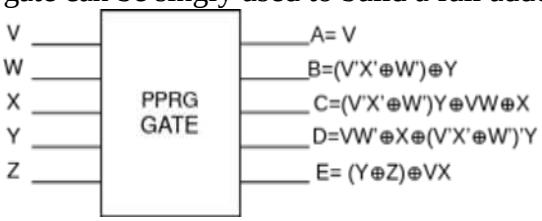
IV. 5*5 Reversible logic gates

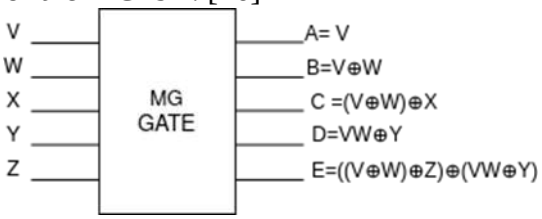
PPRG GATE:

Parity preserving reversible gate is one through which means one of its inputs is also an output.It is a universal gate. The input vector is Iv={V,W,X,Y,Z} and the output vector is Ov={V, (V'X'⊕W')⊕Y, (V'X'⊕W')Y⊕VW⊕X, VW'⊕X'⊕(V'X'⊕W')'Y, (Y⊕Z)⊕VX}. P2RG gate can be singly used to build a full adder and full subtractor.[26]



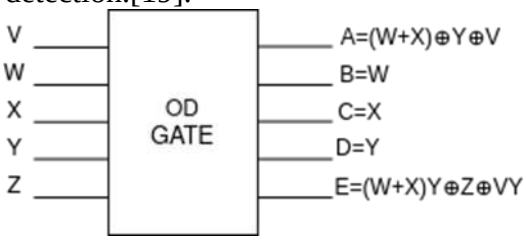
MG GATE:

Morrison Gate is programmable reversible logic gate.The input vector is Iv={V,W,X,Y,Z} and the output vector is Ov={V, V⊕W, (V⊕W)⊕X,VW⊕Y, ((V⊕W)⊕Z)⊕(VW⊕Y)}. The quantum cost of the MG is 7. [16]



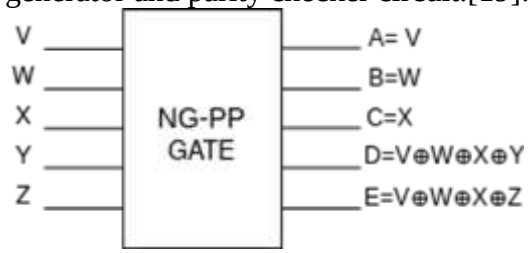
OD GATE :

The input vector is Iv={V,W,X,Y,Z} and the output vector is Ov={(W+X)⊕Y⊕V, W, X, Y, (W+X)Y⊕Z⊕VY }. Overflow Detection gate has quantum cost of 10. OD gate is used for overflow detection.[19].



NG-PP :

The input vector is Iv={V,W,X,Y,Z} and the output vector is Ov={V, W, X, V⊕W⊕X⊕Y, V⊕W⊕X⊕Z }. The quantum cost of NG-PP gate is 5 (Misra et al ., 2017). It is used as parity generator and parity checker circuit.[19].



HG-PP GATE :

The input vector is Iv={V,W,X,Y,Z} and the output vector is Ov={V⊕X⊕Z, W⊕X, X, Y⊕Z, Z }. The quantum cost of the HG-PP gate is 4 .

The number of 1's in input and output are the same. HG-PP gate is used to design hamming code.[19]

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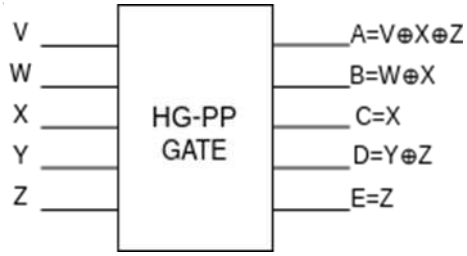

V. 6*6 Reversible logic gates

BSCL GATE :

Binary Coded Decimal Subtraction Correction gate is used to either find correction logic for BCD subtraction or to pass same data to the output depending on the control signal (Rashmi et al ., 2011). The input vector is Iv={U,V,W,X,Y,Z} and the output vector is Ov={Z⊕Y , Z'U+Z[Y'{U⊕(V+W)}+Y{U+VWX}], Z'V+[Y(V⊕W)+Y(V⊕WX)],Z'W+ZY'W+ZY(W ⊕X), Z⊕X, Z}. Here Z is the control signal, if Z is equal to 0,U,V,W,X,Y is passed as it is to the output. If Z is equal to 1 and if Y is equal to 0 then B, C, D and E is the nines complement of the input binary number U,V,W and X. If Y is equal to 1 then binary number 0001 is added to UVWX to get the valid corrected subtraction result.[19]

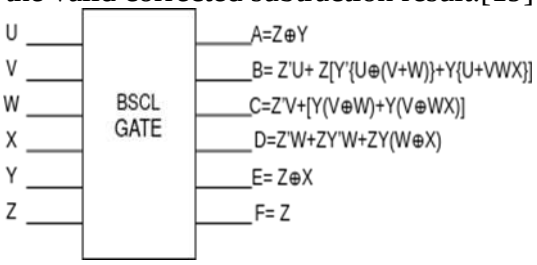

Table 1. Reversible logic gates Summary

SR.NO	GATE NAME	JANTUMCOST	APPLICATION
1	CNOT/ Feynman Gate	1	Duplication of output, inverter
2	Toffoli Gate	5	Universal logic gate
3	Fredkin Gate	5	Swap operation
4	Peres Gate	4	Subtractor
5	Double Feynman Gate	2	Parity preserving
6	BJN Gate	5	Universal logic gate
7	RMUX1 Gate	4	Multiplexer
8	TRG ate	4	Subtractor
9	NEW Gate	4	Adders
10	SAM Gate	4	Flipflop Implementation
11	NFT Gate	4	Parity preserving
13	RC-1Gate	5	Comparator
14	UPG Gate	4	Universal logic gate
15	YAG Gate	4	AND, OR, XNOR and EXOR Implementation

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16	RMUX2 Gate	4	Multiplexer
17	HAS Gate	5	Subtractor
18	Double Peres Gate	6	Adders
19	MRG Gate	6	AND, OR, XNOR and EXOR Implementation
20	SAYEM Gate	6	Flipflop Implementation
21	TSG Gate	14	Adders
22	DKG Gate	17	Adders
23	SCL Gate	Not Defined	Six correction to get actual BCD sum
24	BVF Gate	2	Extracting necessary outputs to meet fan-out
25	ALG Gate	11	Adders
26	PPHCG Gate	6	Hamming error coding and detection.
27	IG Gate	6	AND, OR, XNOR and EXOR Implementation
28	MKG Gate	13	Universal logic gate
29	BME Gate	5	Multiplier implementation
30	PTR Gate	Not Defined	Adders
31	PAOG Gate	6	Universal logic gate

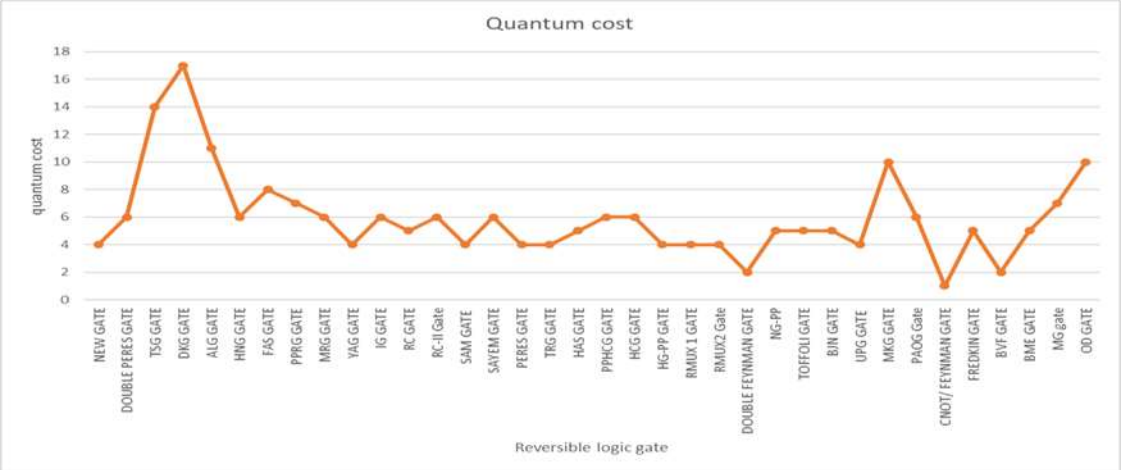

Fig 1. Comparison of quantum cost of reversible logic gates

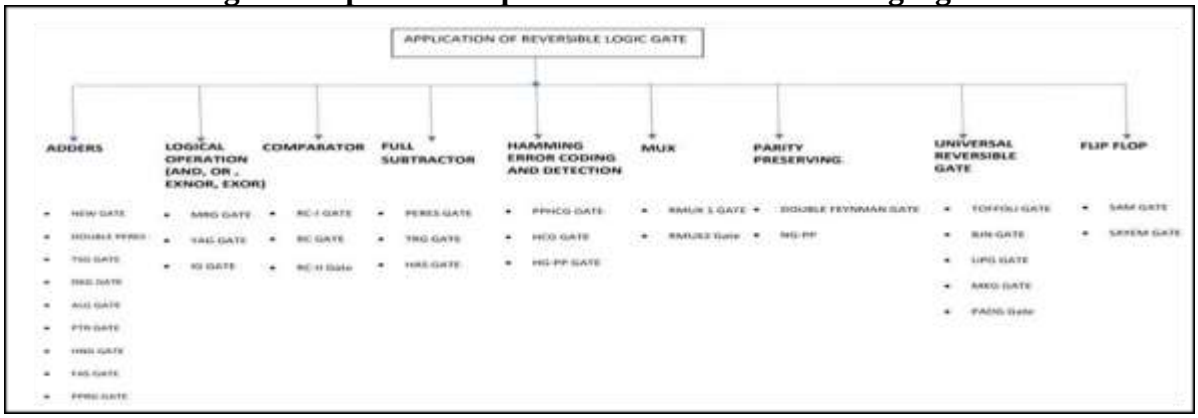

Fig 2. Application of reversible logic gate

VI Application of Reversible Logic Gates

The advantages of reversible logic gates made it very popular for its usage in several applications as listed in figure 2. Reversible gates have been widely used for design of Binary and BCD adders, Multipliers, Sequential circuits, Arithmetic Logic Unit, Vedic Multipliers etc.

CONCLUSION:

In this literature survey, reversible logic gates and their applications from various research papers implemented til date are summarized. As reversible logic is attracting attention due to its advantages over CMOS technology, this overview of the reversible logic gates will help the designers implement complex digital circuits using reversible logic.

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