



AN EFFECTIVE CONTROL AND PULSE GENERATION STRATEGY FOR MODIFIED BRIDGELESS PFC CONVERTER

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ABSTRACT

The increasing adoption of electric vehicles (EVs) necessitates efficient and reliable charging solutions. Power Factor Correction (PFC) plays a crucial role in EV charging systems to maintain high power quality and comply with international standards. A Discontinuous Conduction Mode (DCM) based Bridgeless PFC converter has been developed to enhance the efficiency and performance of EV chargers. By eliminating the traditional diode bridge rectifier, the proposed converter architecture reduces conduction losses and boosts overall system efficiency. Operating in DCM simplifies control strategies, reduces electromagnetic interference (EMI), and enables a more compact design, making it particularly suitable for EV charging applications. The paper involves matlab simulation to validate the converter's performance under various operating conditions. In addition, a modified circuit is introduced that mitigates high current stress, thereby improving system reliability and efficiency. Simulation results also validate the significant improvement in power factor correction, output voltage stability, and overall performance.

Keywords:

Electrical vehicle, Buck-Boost converter, Bridgeless topology, Power factor correction, Discontinuous conduction mode operation.

I. Introduction

Electric vehicles have dramatically changed the transportation sector by providing an alternative that is environmentally friendly and efficient compared to traditional gasolinepowered vehicles [1]. They are a solution to reducing carbon emissions and improving air quality, which will positively contribute to environmental sustainability. Long-range EVs with charging infrastructure have gained popularity, but there is still a considerable market for low-range EVs for specific purposes. Often being called micro-mobility solutions [2], these cars are designed to cope with city conditions and for short commutes. However, their low range demands innovative charging strategies for continuous operation. Low range EV charging applications includes different charging technologies, infrastructure requirements, and potential future developments to ensures a smooth integration of EVs into daily life. Conventional bridge topologies, widely utilized in EV onboard chargers [3], typically employ a diode bridge rectifier to convert the AC input voltage to DC. Such a configuration is simple but at the cost of increased conduction losses [4] due to the voltage number of components and complex control strategies associated with conventional bridge topologies contribute to higher system costs and reduced efficiency. In bridgeless topologies, the diode bridge rectifier is absent. It makes use of the AC input voltage directly. It reduces conduction losses to a great extent. This results in improved efficiency and

increased power density. The reduced component count also helps in simplifying the control strategy and reduces the overall system cost. Although several advantages are found in bridgeless topologies, careful design considerations are made to mitigate challenges such as increased current stress on the switches and the potential for increased EMI. Bridgeless DCM-based power factor correction (PFC) [5] is expected to be more dominant in electric vehicle (EV) charging applications, as it has shown significant advantages in terms of efficiency, simplicity, and a lower number of components. Unlike the conventional bridged PFC converters, which use a diode bridge at the input, the bridgeless design does not include this component, thus greatly reducing conduction losses and enhancing power density. Moreover, this converter achieves natural power factor correction without the need for extra sensors to measure input voltage and current by working in Discontinuous Conduction Mode (DCM). Thus, this results in lower costs and a less complex control structure. The DCM-based bridgeless power factor correction (PFC) is highly efficient and compact and requires only one sensor and a simple control loop. This design not only increases robustness and reduces cost but also alleviates operational issues. In addition, the exclusion of the bridge rectifier greatly reduces power losses and effectively mitigates challenges associated with thermal management, leading to improved overall efficiency and power density. In this operating mode, the input current is carefully aligned with the input voltage, achieving a power factor that is close to unity. This method simplifies electric vehicle (EV) charging systems by removing the need for complicated feedback mechanisms, making it easier to follow International Electrotechnical Commission (IEC) standards on harmonic limits drop across the diodes. In addition, the increased

II. Conventional Topologies

There are many existing topologies [6], [7] for DCM-based bridgeless PFC converter. It includes Bridgeless boost PFC, Dual boost PFC, Semi bridgeless PFC, Totem pole PFC, Interleaved bridgeless PFC converter, etc. Let us go to the details of each one of these topologies, highlighting its advantages and disadvantages.

2.1 Bridgeless Boost PFC converter

This configuration is made up of two switches that are controlled by identical gating pulses. By not having an extra gate driver circuit, the efficiency and power density of the converter are enhanced compared to those bridgeless boost PFCs with individual driver circuits. It also eliminates the heat management issue of the diode bridge rectifiers. However, there are possibilities for the introduction of EMI issues related to this circuit. Since the input line is floating against the ground, it is not feasible to feel the input voltage without an optical coupler or a low-frequency transformer. Again, intricate circuitry is also required to monitor the input current.

2.2 Dual Boost PFC Converter

In dual boost PFC, gates of MOSFET switches in [8] are decoupled. One of the switches is ON for every half cycle of the input supply. Under light load conditions, the conduction losses can be minimized until the voltage drop across the MOSFET body diode equals the voltage drop across the MOSFET channel because, after this point, more current passes through the body diode. The light load efficiency enhancement is obtained at the cost of extra driver circuits.

2.3 Semi Bridgeless Converter

For semi bridgeless converter, two more slow diodes are introduced. Two such diodes short the input to the ground of the PFC, and thereby, they overcome the EMI problem [9]. Losses during conduction in slow diodes are minimum due to the fact that current doesn't flow back via them all the time. Two boost converters will operate alternately in the positive and negative half cycle of the supply. It can be sensed through a chain of voltage dividers. Low usage of inductors and devices lowers the power density and increases the cost of the converter with respect to traditional boost PFC.

2.4 Totem pole Bridgeless PFC converter

In a totem pole bridgeless PFC converter, Only one low frequency diode and one switch are conducting at a time in a totem pole bridgeless PFC converter and therefore will have the lowest conduction losses.

It contains a greater efficiency and power density than other converters. The speed of recovery of the body diode in MOSFET is so low that both the switches will conduct at once, damaging circuits. Hence, a fast-recovery MOSFET has to be implemented.

2.5 Bridgeless Interleaved Converter

Bridgeless Interleaved converter uses four MOSFETs (two switches in pairs) and four fast diodes. The gating signals of two switch pairs are 180 degrees out of phase. Due to interleaving structure of the circuit, current stress in switches is low and therefore reliability and fault tolerance can be enhanced. Its highest efficiency is 98.5 % at 1.2kW load and 70 kHz switching frequency [10], [11], [12]. The main disadvantage of the bridgeless interleaved converter is that it is costly due to the larger number of magnetic components.

III. Design and Analysis of DCM based BL-PFC Converter

Fig 1 shows the circuit diagram of the DCM based BL-PFC converter. It includes two back-to-back connected MOSFETs, two diodes, one inductor, a filter circuit, and two electrolytic capacitors. The MOSFETs are configured in a common source arrangement and controlled by a unified gate signal, allowing them to operate as a single switch (S). This converter functions exclusively in boost mode, reverse biasing the output diodes when switch S is turned ON. Only one of the diodes will be conducted in the positive and negative half-cycles. For the positive cycle, D_2 will be conducted and for the negative cycle, D_1 . To analyze the principle of a DCM-based Bridgeless buck-boost PFC converter [13], a positive half cycle is included, and the working of the negative half cycle will be similar to the positive half cycle.

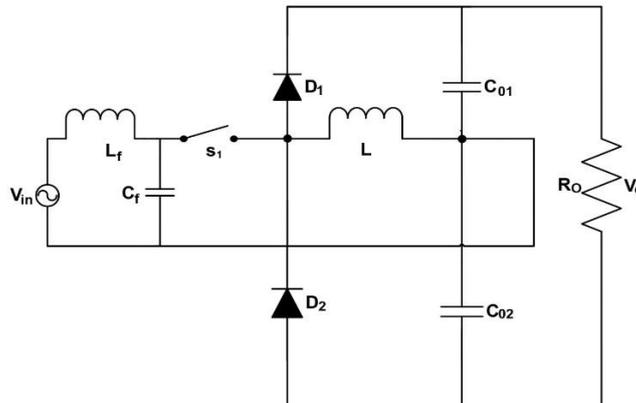


Fig 1. Circuit diagram of BL-PFC converter

4.1. Mode 1

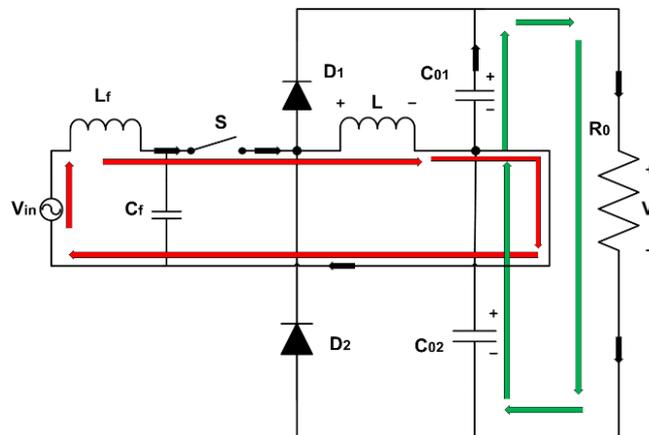


Fig 2. Mode 1 operation for positive half cycle

Fig 2 shows the mode 1 operation of a DCM-based Bridgeless PFC converter. Switch (S) is turned on with a gate pulse. The energy is stored in the inductor L. The output capacitors C_{01} and C_{02} maintain

the voltage across the load. (1) and (2) show that the input voltage is equal to the inductor voltage, and (3) shows the current through the inductor.

$$V_{in}(t) = V_L(t) \quad (1)$$

$$V_{in}(t) = L \frac{di_L(t)}{dt} \quad (2)$$

$$i_L = \frac{V_L(t)}{L} \quad (3)$$

4.2 Mode 2

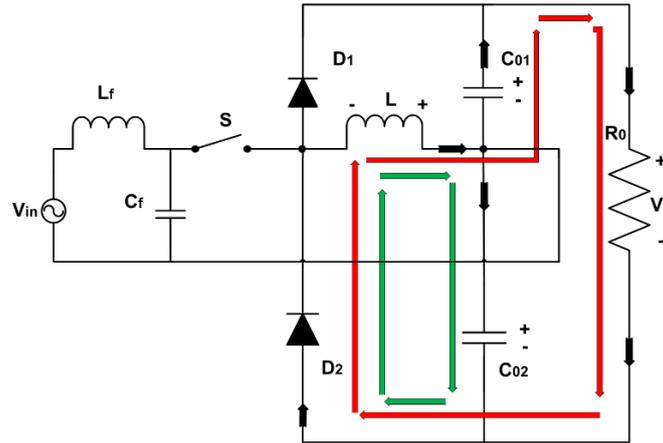


Fig 3. Mode 2 operation of positive half cycle

In Fig 3, when the switch is opened, and the gate pulse is removed, the stored energy in the inductor L begins to de-energize. This process occurs as the inductor transfers its energy to a load through the C_{01} capacitor. During this energy transfer, C_{01} supplies power to the load, ensuring that it continues to operate even as the inductor discharges. During the same time, the C_{02} capacitor is also charged.

$$i_L(t) = i_{LPK} - \frac{V_0}{2L} \quad (4)$$

4.3 Mode 3

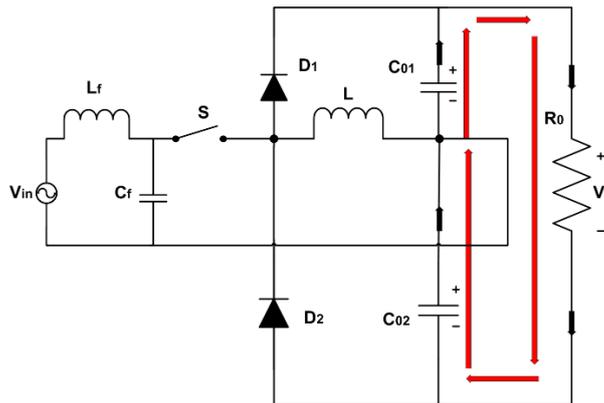


Fig 4. Mode 3 operation of positive half cycle

$$i_L = 0 \quad (5)$$

Fig 4 shows the mode 3 operation of the DCM-based Bridgeless PFC converter. All switching components are in their off state. This interrupts the current flow through the inductor (L). The output capacitors, C_{01} and C_{02} , maintain the voltage across the output load. (5) shows the current through the inductor in the mode 3 operation. In Mode 1, the switch is turned ON, resulting in a linear increase of inductor current. During this time, the diode is reverse-biased and does not conduct. The voltage across the inductor, V_{in} , is equal to the input voltage V_g . Mode 2 occurs when the switch is turned OFF. The UGC CARE Group-1

inductor current continues to flow through the diode, causing it to conduct. In this mode, the voltage across the inductor V_{in} becomes equal to the output voltage V_o , and the inductor current gradually decreases. Mode 3 occurs when the inductor current reaches zero before the end of the switching cycle. At this point, both the switch and the diode are OFF, and the inductor current remains at zero until the next switching cycle commences.

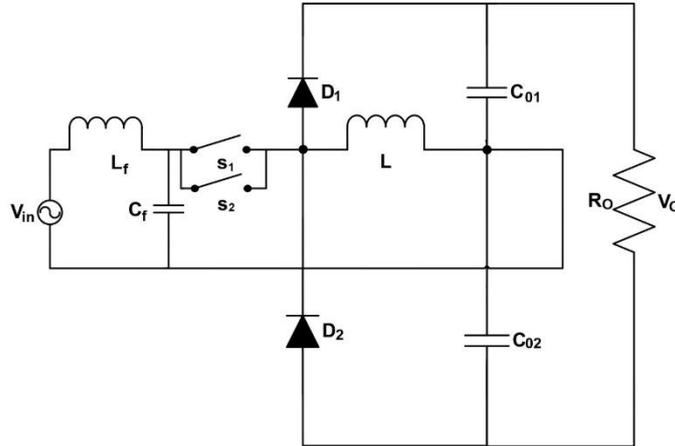


Fig 5. Modified BL-PFC converter

Fig 5 illustrates the Modified Bridgeless PFC Converter, which operates in Discontinuous Conduction Mode (DCM). Each switch is composed of back-to-back connected MOSFETs to prevent reverse current flow. Different gate pulses are applied to switches S_1 and S_2 . During the positive cycle, switch S_2 conducts, and during the negative cycle, switch S_1 conducts. The diode in the system ensures that current flows in only one direction, maintaining unidirectional current flow through the inductor. The design, working, and principle of operation of the modified circuit are the same as that of the unmodified circuit. The only difference is that during the positive half cycle, S_2 conducts, and during the negative half cycle, S_1 conducts. Thus, the rms value of current passing through the switches is reduced, and hence the problem of increased current stress on switches can be rectified.

4.4 Design

a) Load Resistor, R_0

The output power and output voltage are taken as $P_0 = 1000W$ and $V_0 = 800V$

$$R_0 = \frac{V_0^2}{P_0} = \frac{800^2}{1000} = 640\Omega \quad (6)$$

So, the value of the load resistor is set as $R_0 = 640 \Omega$

b) Voltage Gain (M)

The input peak voltage is taken as $V_{pk} = 230V$.

$$M = \frac{V_o}{V_{PK}} = \frac{800}{230} = 3.47 \quad (7)$$

Voltage gain = 3.47

c) Duty Ratio (D)

$$D < \frac{M}{M + 2} = \frac{3.47}{3.47 + 2} = 0.6358 \quad (8)$$

The duty ratio must be less than 63.58% and is set at 62%.

d) Inductors L, L_f

L is the buck-boost inductance and L_f is the filter inductance.

Z_{in} = input impedance, Z_{ch} = characteristic impedance.

$Z_{ch} = Z_{in} = 1$, Z_{in} and Z_{ch} is made equal for maximum power transfer.

$X_L = X_c = Z_{in}$ (to attain resonance condition).

$$Z_{in} = \frac{2L}{D^2 T_s} = \frac{2 \times 35 \times 10^{-6}}{62^2 \times 1 \times 10^{-5}} = 18.21 \Omega \quad (9)$$

$$L < \frac{V_{PK}^2 V_o^2 T_s^2}{4 P_o (V_o + 2 V_{PK})^2} = \frac{230^2 \times 800^2 \times 1 \times 10^{-5}}{4 \times 1000 \times (800 + 2 \times 230)^2} = 5.33 \times 10^{-5} H \quad (10)$$

20% tolerance is applied to L and is taken as 35 μ H.

$X_L = 2\pi f_c L$. Therefore,

$$L_f = \frac{Z_{ch}}{2\pi f_c} = \frac{18.21}{2 \times 3.14 \times 3 \times 10^3} = 0.9 \text{ mH} \quad (11)$$

e) Capacitors C_0, C_f

C_f represents the filter capacitor and C_0 denotes the output capacitor.

Switching frequency, $f_s = 100$ kHz, Switching Time Period, $T_s = \frac{1}{f_s} = 0.00001$ sec.

Taking $Z_{ch} = Z_{in}$ and assuming a cutoff frequency of $f_c = 3$ kHz.

$$X_c = \frac{1}{2\pi f_c} \quad (12)$$

$$C_f = \frac{1}{2\pi f_c Z_{ch}} = \frac{1}{2 \times 3.14 \times 3 \times 10^3 \times 18.21} = 2.9 \mu F \quad (13)$$

$$C_0 = \frac{V_o \times D}{F_s \times R \times V_{0,ripple}} = \frac{800 \times 0.62}{100 \times 10^3 \times 640 \times 40} = 1400 \mu F \quad (14)$$

IV. Results And Discussion

6.1 Simulation Results

Fig 6 shows the open loop control and pulse generation circuit of a modified bridgeless PFC converter. In this, a zero crossing detector and pulse generator are used to generate pulses for two pairs of switches S_1 and S_2 . The output of the zero crossing detector is [SA] and the output of the pulse generator is [SB]. The product of [SA] and [SB] is given to the S_2 . ie, the lower pair of switches. So, the lower pair of switches conducts during the positive half-cycle. The [SA] is inverted using an inverter and the product of [SA]' and [SB] is given to S_1 . ie, to the upper layer of switches. So, the first pair of switches conduct during the negative half cycle. Fig 7 shows the input voltage and input current waveforms obtained from the open loop simulation of the modified BL-PFC converter. From the figure, it is clear that the power factor has been corrected accurately. Fig 8 shows the gate signals and current through the switches. G1 is the gate signal given to switch S_1 and G2 is the gate signal given to switch S_2 . The rms current on each switch is reduced by paralleling of switches. But still, the issue of overshoot persists during startup.

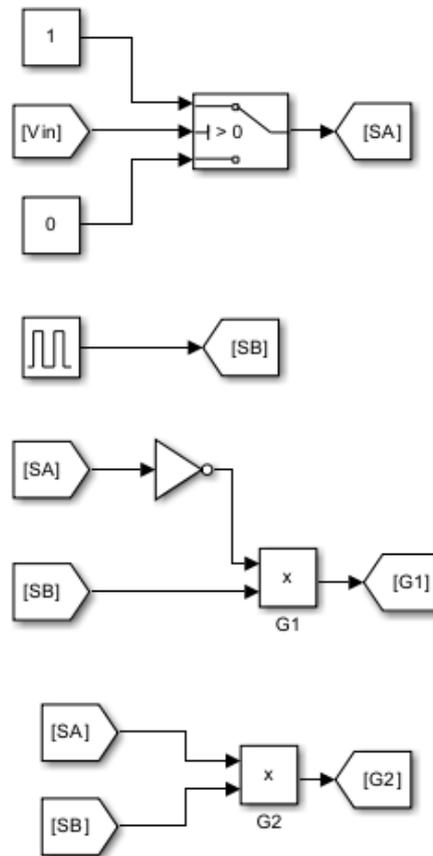


Fig 6. Open Loop control and pulse generation circuit

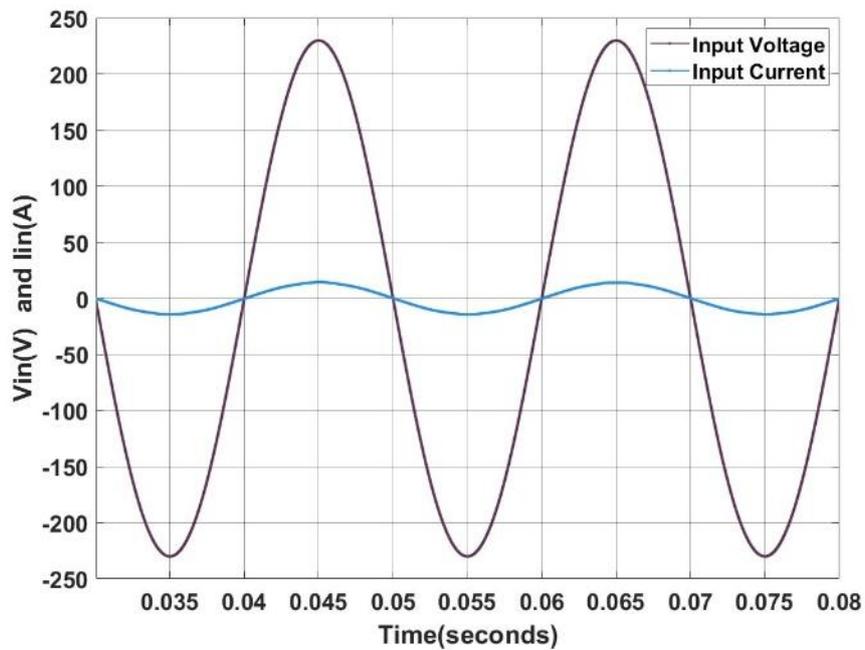


Fig 7. Input current and input voltage

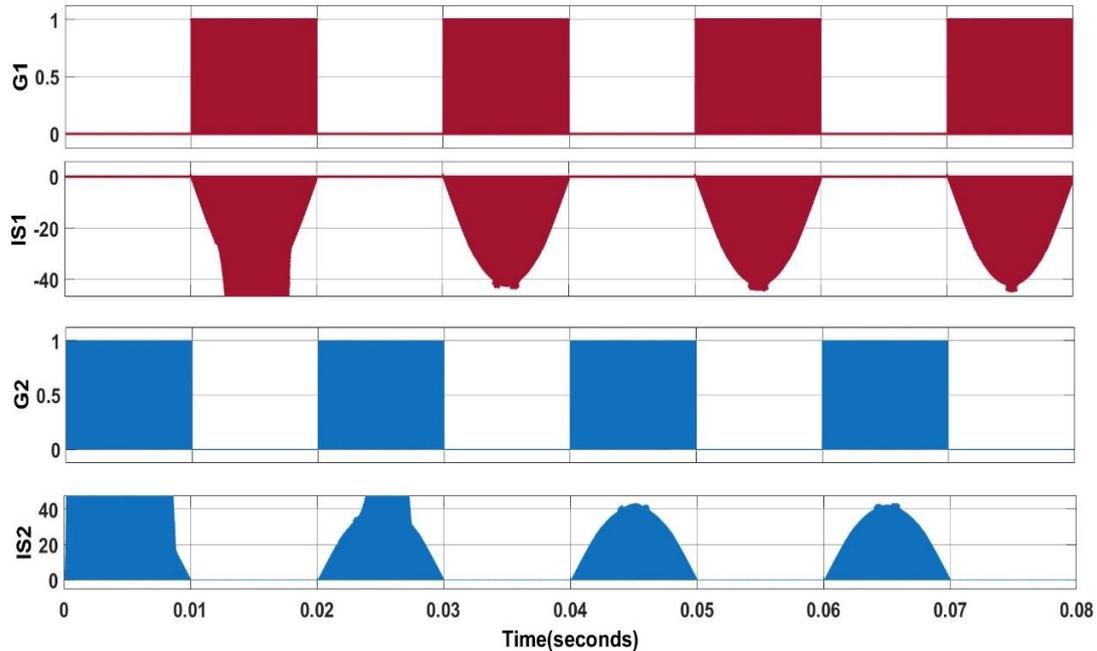


Fig 8. Gate signals and current through switches

Fig 9 shows the closed loop control and pulse generation circuit. A ramp function is used to increase the duty ratio from 0 to 62% slowly instead of giving a 62% duty ratio directly. During the start-up of the converter, the output voltage is zero or very low values. So, the error becomes a very high saturated value. It leads to sudden voltage buildup and capacitor charges to tremendously very high values. It takes much time to minimize that. As a remedy for this, a soft switching technique is employed here. By using ramp function, voltage increases slowly and avoids overshoots. During loaded conditions, the PID controller and limiter together manage high-voltage buildups. The output voltage is compared with reference voltage. If the output voltage is greater than the reference voltage, the output will be 'HIGH'. A step function is given for 0.02 seconds so that during startup time, the product block output is zero. The PWM generator generates a pulse with a switching frequency of 100 kHz according to the duty cycle generated by the PID controller. The output of the PWM generator is given to the switch block which acts like a zero crossing detector. During startup, the upper part that involves the ramp function and the PWM generator works, and after that the remaining part works. Here, the simulation is performed considering load variations by adding a variable load block. Fig 10 shows the input voltage and input current obtained from closed loop simulation. The power factor correction has been obtained efficiently. Fig 11 shows the gate pulses and current through switches. It is visible that no overshoots are occurring there. Current stress is also reduced on the switches. Fig 12 shows the result of THD obtained from closed-loop simulation of the modified circuit. The desired THD value is less than 5% and the THD obtained from closed-loop simulation is 4.65% which is less than 5%. So, it is within the range. Table I shows the different parameter values obtained from closed-loop simulation of modified and unmodified bridgeless PFC converter. The major changes are observed in current through switches and THD. The THD obtained from the simulation of the modified circuit is 4.65 % which is less than that of the unmodified circuit. The output voltage obtained from the modified circuit is 802V. It is close to the value of reference voltage 800V. But in case of unmodified circuit, the output voltage obtained is 867.5V. So, the modified circuit has better control of voltage. The increased value of output current can be controlled if we incorporate current control techniques to it.

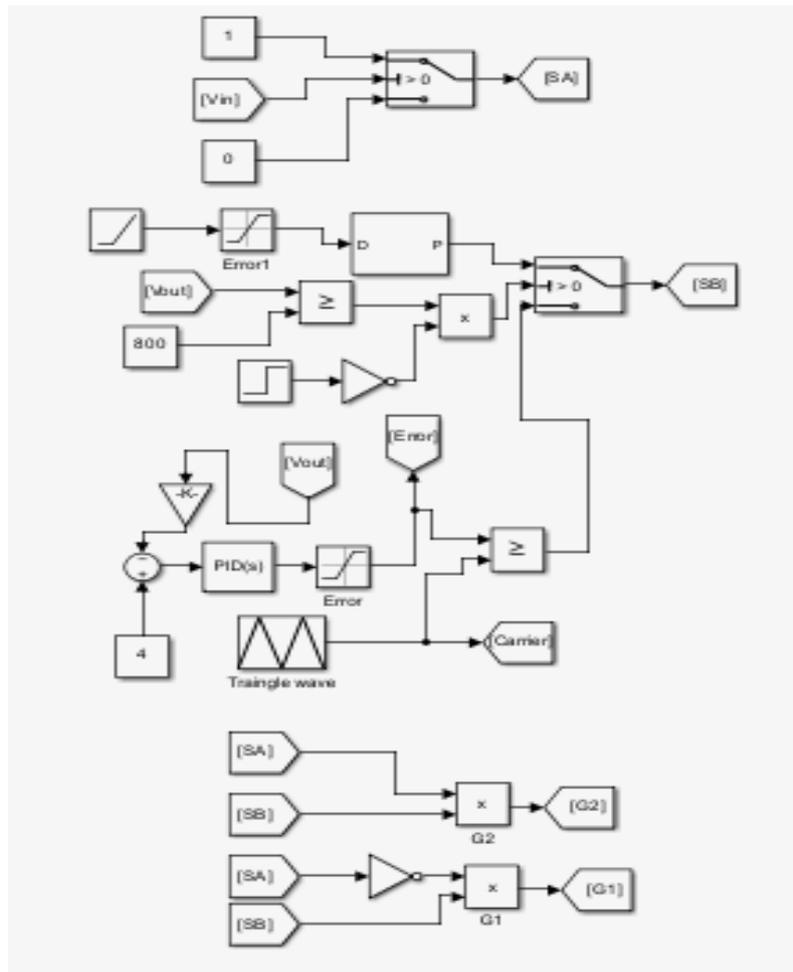


Fig 9. Closed loop control and pulse generation circuit

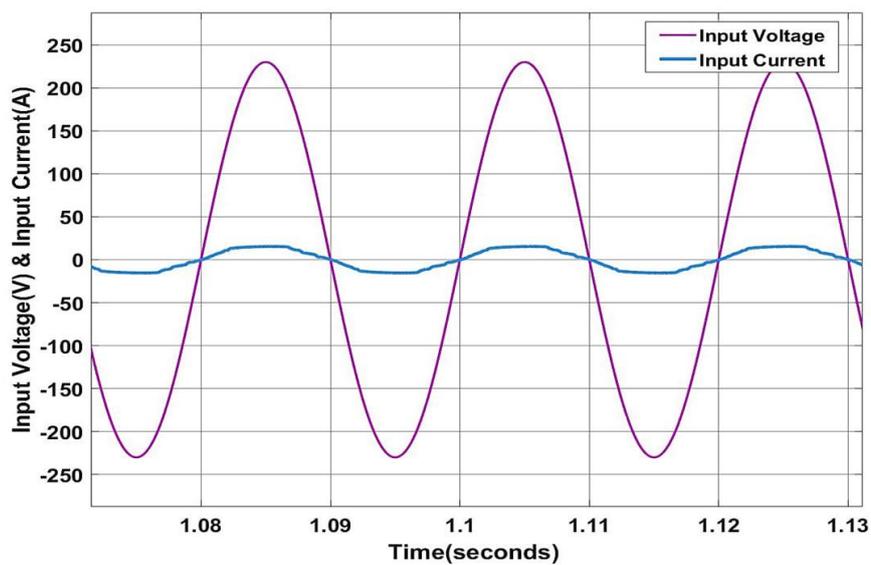


Fig 10. Input voltage and input current waveforms

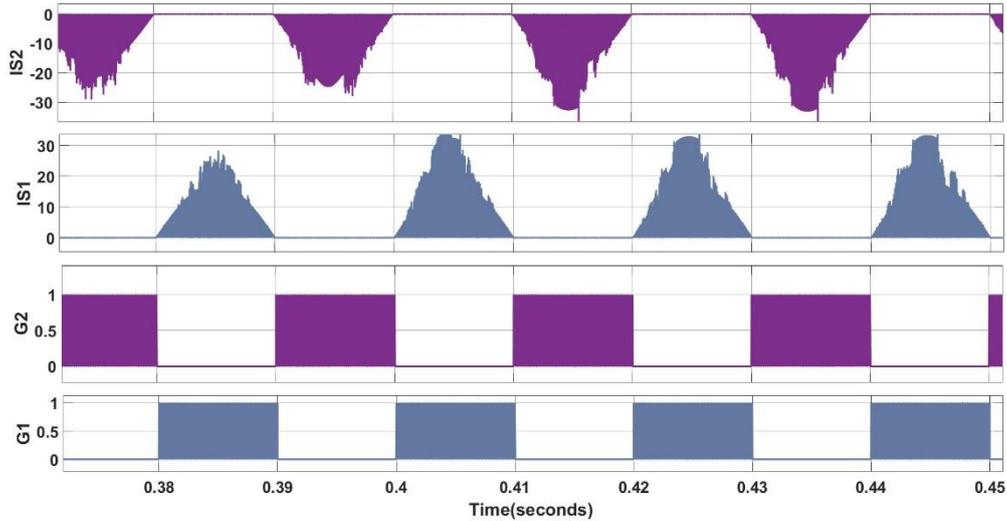


Fig 11. Gate pulses and current through switches

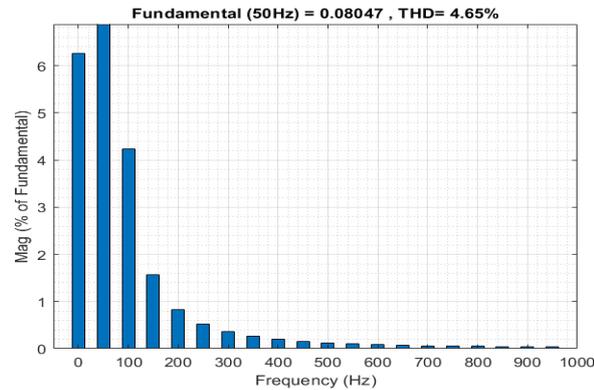


Fig 12. THD obtained from modified circuit

TABLE I. Comparison of modified and unmodified BL-PFC converters

Parameter	Unmodified Circuit	Modified Circuit
Input Voltage	230V	230V
Input Current	13A	13A
Current Through Switch	33A peak to peak	0-33A during one half cycle 0A during next half cycle
Voltage Across Switch	680V	650V
Current Through Inductor	40A	42A
Voltage Across Inductor	440V	420V
THD	4.68%	4.65%
Output Voltage	867.5V	802V
Output Current	1.04A	2A

V. Conclusion

The application of a Discontinuous Conduction Mode (DCM)-type bridgeless power factor correction (PFC) converter is an extremely efficient and compact solution for electric vehicle (EV) charging systems. With the removal of the traditional diode bridge rectifier, the design minimizes conduction losses and maximizes overall system efficiency. The converter utilizes open-loop and closed-loop control techniques to maximize performance. The open-loop control method employs a pulse generation circuit and zero-crossing detector to provide precise switching of the MOSFETs, thus



enhancing power factor correction as well as minimizing switching losses. Issues like transient overshoot and current switch stress are found in this mode. In order to resolve these issues, a closed-loop control method is implemented, which includes the application of a ramp function and a PID controller. The ramp function guarantees a smooth ramp-up of the duty cycle, thereby suppressing startup overshoots, while the PID controller dynamically adjusts the duty ratio through real-time output voltage feedback, guaranteeing stable operation under dynamic load conditions. Simulation results confirm that the system registers near-unity power factor, voltage regulation stability, and low total harmonic distortion (THD). Further, the modified topology also lessens current stress on switching elements to further promote overall reliability. In this paper, it has been proven that the DCM-based bridgeless PFC converter with its state-of-the-art control and pulse generation techniques holds high potential in augmenting EV charging infrastructure efficiency and reliability and conformity to power quality standards.

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