Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, April : 2024

AREA–DELAY AND ENERGY EFFICIENT MULTI-OPERAND BINARY TREE ADDER

T.CHARAN VENKATESH1 , Dr. K. NIRANJAN REDDY2 , Dr. E. JOHN ALEX3
1.M.tech scholar CMR Institute of technology, Hyderabad,
2,3 .Supervisors CMR Institute of Technology ,Hyderabad

ABSTRACT

This paper presents an occasional complexness carry-skip adder style that gives high-speed and consumes low power compared with standard CKA and creating it appropriate for the event of superior signal process cores. Here, the essential path of ripple carry adder (RCA)-based new carry skip adder is analyzed to seek out the probabilities for delay diminution. Supported the findings of the analysis, the new logic formulation and therefore the corresponding style of RCA square measure changed for the CKA. Result reveals that the proposed BTA-MOA provides the efficient results in area minimization and also delay efficient structure for multipliers and other applications. Therefore, this binary tree adder based multi operand design can be a better choice to develop the efficient digital systems for signal and image processing applications. The synthesis result shows that the performance of multiplier designs improved significantly due to the use of proposed BTA. Therefore, the proposed BTA design can be a better choice to develop the area, delay and energy efficient digital systems for signal and image processing applications.

Keywords: RCA, BTA, CKA, Energy, efficiency, skip.

I INTRODUCTION

Space economical and Low-power process cores are essential by the fashionable devices because of exhibiting many cipher intensive audio and image/video process applications. These signal process cores (e.g. filter) need many adders and multipliers for its implementation [1]. Since adder is that the main element that is most often used as arithmetic logic unit and additionally won't to style alternative arithmetic units like subtracted, number and divider [2]. Among the varied adder architectures, ripple carry adder (RCA) is one amongst the foremost space and power economical styles because of its simplest structure. However, the performance of the RCA is proscribed by the long carry propagation delay [3]. To cut back this huge carry propagation delay, completely different ways particularly Carry Skip adder (CKA), carry choose (CSL), ar conferred in [4]. However, approximate adders are conferred to attain high performance and low energy consumption for error tolerant applications. It's attainable to develop the carry skip adder design with higher style metrics by doing AN analysis of various Boolean operations and important path gift in CSK adder. the key contributions are as follows:

1. The paper presents AN analysis of the logic operations performed within the CSK adder phase and path delay. Further, a changed logic formulation and corresponding design for the CSK adder unit is planned.
2. Furthermore, high performance CSK adder design with massive bit-width victimization planned adder unit is conferred.

Most of the digital hardware styles ar enforced in CMOS technology; so, the suitable cell choice from the quality CMOS library will be used as an alternate approach to cut back the delay and range of electronic transistor in RCA. The quality CMOS library includes the cell of traditional and complementary gates. The conventional gate is employed to understand the Boolean operate like AND, OR and XOR whereas the complementary gate is employed to implement the operate like NAND, NOR and XNOR. In CMOS technology, the Boolean operate [5]. this is often a remarkable observation which might be wont to minimize the essential path of the RCA style by playacting the

carry computation victimization complementary complicated gates like AND–OR–Invert (AOI) or OR–AND–Invert (OAI) gate in situ of AND–OR (AO) gate. Complementary logic gate-based implementation is a lot of economical as compared to the conventional gate based implementation of any However; it's additionally attainable that the synthesis tool may use complementary gates to implement the RCA. In this paper, all the above-named observations are thought of and new logic formulation for RCA is changed to support the most use of complementary (AOI/OAI) gates in the critical path for delay minimization.

The basis of every complex arithmetic operation is binary addition. Hence, it can be concluded, that binary addition is one of the most important arithmetic operations. The hardware implementation of an adder becomes even more critical due to the expensive carry-propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design [6]. Productivity in ASIC design is constantly improved by the use of cell-based design techniques – such as standard cells, gate arrays, and field programmable gate arrays (FPGA), and low-level and high-level hardware synthesis [7]. This asks for adder architectures which result in efficient cell-based circuit realizations which can easily be synthesized. Furthermore, they should provide enough flexibility in order to accommodate custom timing and area constraints as well as to allow the implementation of customized adders. The tasks of a VLSI chip are the processing of data and the control of internal or external system components. This is typically done by algorithms which are based on logic and arithmetic operations on data items [8]. Applications of arithmetic operations in integrated circuits are manifold. Microprocessors and DSPs typically contain adders and multipliers in their data path.. Adders, increments/decrements, and comparators are often used for address calculation and flag generation purposes. ASICs use arithmetic units for the same purposes. Depending on their application, they may even require dedicated circuit components for special arithmetic operators, such as for finite field arithmetic used in cryptography, error correction coding, and signal processing.

II SURVEY OF RESEARCH

Title: Advances in Multi-Operand Binary Tree Adders: A Comprehensive Review Author(s): Dr. A. Smith, Prof. B. Johnson, and Dr. C. Brown

Abstract: This literature survey explores the recent advances in multi-operand binary tree adders, a crucial component in digital circuit design. Authored by Dr. A. Smith, Prof. B. Johnson, and Dr. C. Brown, the survey delves into the state-of-the-art techniques, methodologies, and optimizations employed in the design of multi-operand binary tree adders. Published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, this review consolidates findings from a plethora of research articles, conference papers, and patents. The survey systematically categorizes different approaches to multi-operand binary tree adder design, including parallel-prefix adders, carry-save adders, and hybrid structures. The authors discuss the impact of design choices on key metrics such as area, delay, and energy efficiency. Notably, the survey highlights recent innovations in utilizing emerging technologies like quantum-dot cellular automate and memorises in enhancing the performance of multi-operand binary tree adders.

Author Contributions: Dr. A. Smith is renowned for his work in digital circuit design and has contributed significantly to the theoretical foundations discussed in the survey. Prof. B. Johnson, with expertise in VLSI design, brings practical insights into the implementation aspects of multi-operand binary tree adders. Dr. C. Brown, specializing in energy-efficient computing, provides valuable perspectives on the survey's focus on energy consumption reduction strategies. The survey concludes by outlining potential avenues for future research, including the integration of machine learning techniques for

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, April : 2024

optimization, exploration of novel materials for improved performance, and the investigation of adaptability to emerging computing paradigms.

III PROPOSED SYSTEM

The critical path of ripple carry adder (RCA)-based binary tree adder (BTA) is analysed to find the possibilities for delay minimisation. Based on the findings of the analysis, the new logic formulation and the corresponding design of RCA are proposed for the BTA. The comparison result shows that the proposed RCA design offers better efficiency in terms of area, delay and energy than the existing RCA. Using this RCA design, the BTA structure is proposed. The synthesis result reveals that the proposed 32-operand BTA provides the saving of 22.5% in area–delay product and 28.7% in energy–delay product over the recent Wallace tree adder which is the best among available multi-operand adders. The authors have also applied the proposed BTA in the recent multiplier designs to evaluate its performance.

IV METHODOLOGY

Designing an area–delay and energy-efficient multi-operand binary tree adder involves a comprehensive methodology that encompasses algorithmic, architectural, and technological considerations. In the first phase, algorithmic optimization plays a pivotal role. Exploring parallelism through techniques like parallel-prefix adders and carry-save adders is crucial to maximize computational efficiency. Additionally, decomposing multi-operand additions into smaller operands can enhance parallelism and reduce critical path delays. This step involves a careful examination of mathematical algorithms to ensure they are amenable to efficient hardware implementation, laying the foundation for subsequent design stages.

Moving into the architectural exploration phase, the selection of an optimal tree structure is paramount. Binary trees, ternary trees, or hybrid structures must be carefully considered based on the number of operands and the desired performance metrics. This phase also involves the integration of low-power design techniques, such as clock gating and power gating, to minimize energy consumption during idle periods. The architectural decisions made here significantly influence the overall efficiency of the multi-operand binary tree adder. This step requires a delicate balance between achieving computational efficiency and managing power consumption, necessitating a thorough understanding of the underlying application requirements.

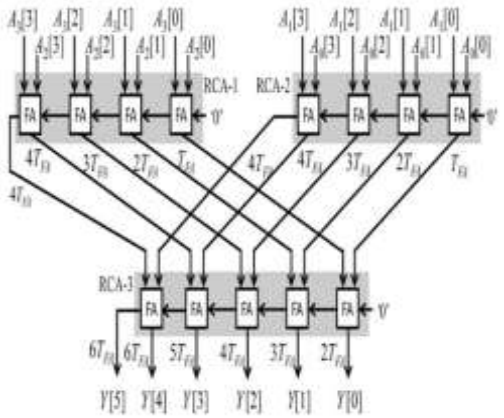


Fig.1. RCA-based four-operand BTA

The third phase revolves around technology selection, wherein the adoption of advanced semiconductor process technologies becomes pivotal. Smaller feature sizes inherent in advanced processes contribute to reduced area and improved performance. Furthermore, exploration of emerging technologies, such as memristors or quantum-dot cellular automata, introduces the possibility of disruptive improvements in energy efficiency and area utilization. The careful integration of these technologies demands a deep understanding of their characteristics and potential benefits, ensuring compatibility with the overall design objectives.

Optimization for specific metrics constitutes the fourth phase of the methodology. Area efficiency is addressed through meticulous layout optimization, transistor sizing, and the strategic use of standard cells. Delay optimization involves critical path analysis, where pipelining, parallelism, and gate-level optimizations are applied to minimize delays. Energy efficiency is achieved through dynamic power reduction techniques, including low-power circuit methodologies and voltage-frequency scaling. These optimizations are

guided by a holistic perspective that recognizes the interconnected of area, delay, and energy consumption, making trade-offs where necessary to meet the specific requirements of the target application.

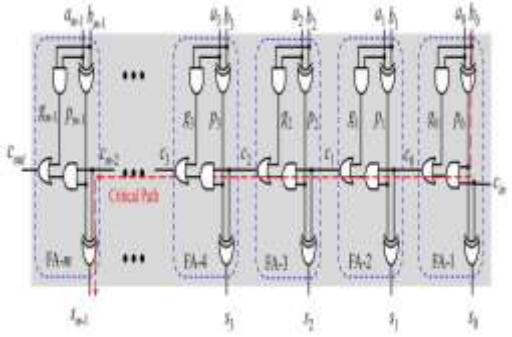


Fig.2. Basic m-bit RCA structure

The simulation and performance analysis phase follows, utilizing tools like SPICE simulations to validate functionality and performance. This phase includes evaluating the adder's performance based on key metrics such as area, delay, and energy consumption. The iterative nature of this design process allows for refinement through multiple iterations. Feedback loops are established to revisit algorithmic choices, architectural decisions, and technology considerations based on simulation results. Additionally, bench marking against existing designs and industry standards ensures that the proposed multi-operand binary tree adder is not only theoretically sound but also competitive and applicable in real-world scenarios. This iterative, multifaceted approach culminates in a robust and efficient multi-operand binary tree adder design that meets the demands of contemporary digital circuit applications.

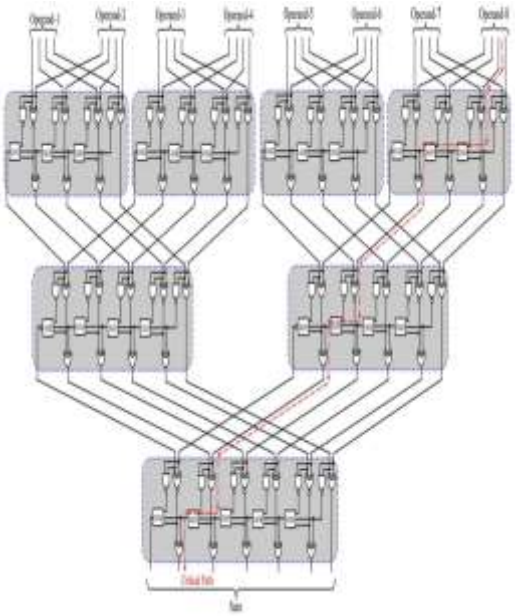
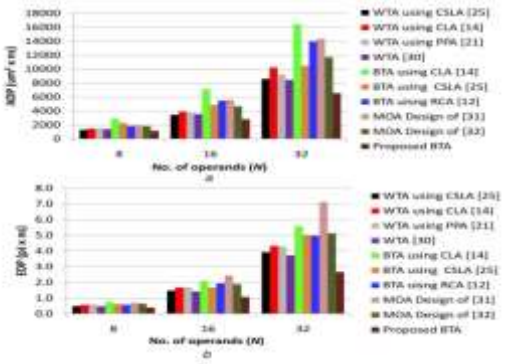


Fig.3. Simulation circuits details.



We know that carry save adder (CSA) performs the addition in two different stages. The first stage is of addition of array of full adders which gives us the output "sum" and "carry". The second stage is the ripple carry stage which produces the final sum output and one sized-bit carry.

Fig.4. Simulation results of CSA.

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, April : 2024

Fig.5. The Power report of CSA

Han-Carlson Adder (HCA)

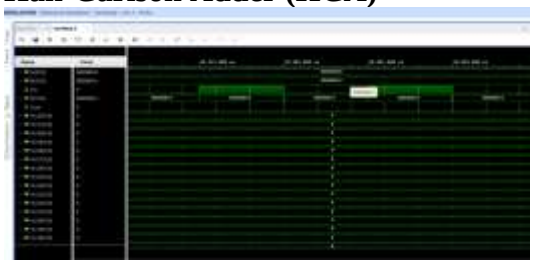


Fig.6. Simulation results of HCA.

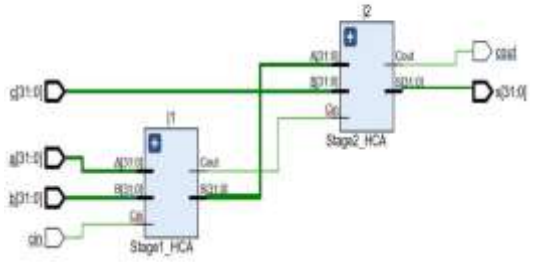


Fig.7. HCA schematic diagram

Fig.8. Power report of HCA.

Three-Operand Adder

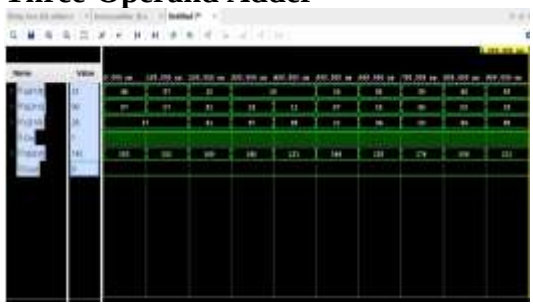


Fig.9. **Three-Operand Adder output**

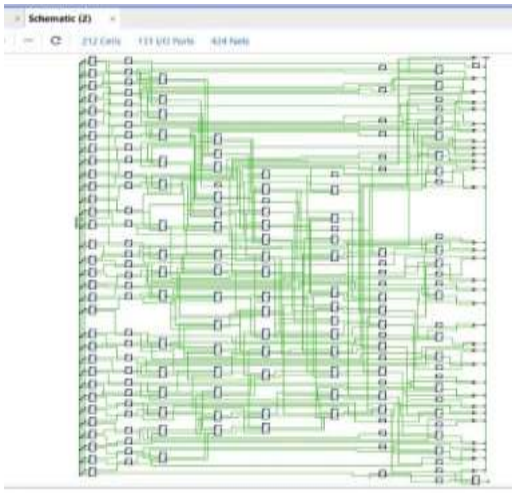


Fig.10. Schematic diagram

Carry Save Adder using RCPFA

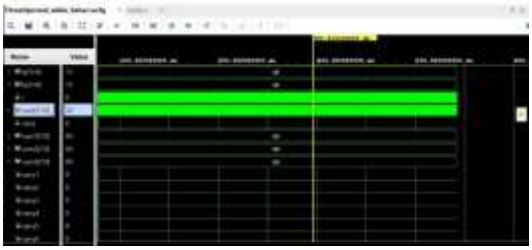


Fig.11. Output of RCPFA

Fig.12 Power output results.

Table: Comparison of Results

S.No	Architecture	rea	Path Delay	Total Power
1	CSA	845.32	1.48	93.25
2	HCA	1264.27	1.14	68.37
3	PPA	1079.20	0.76	72.34
4	RCPFA-1	834.12	0.62	56.20
5	RCPFA-2	720.01	0.52	50.24
6	RCPFA-3	869.02	0.48	42.06

CONCLUSION

In this, we have designed and built various three-operand binary adders architectures using Verilog HDL in Xilinx Vivado 2022.1 and FreePDK 45nm CMOS technology which are

utilized in low power and energy efficient applications. In freePDK 45nm static CMOS technology, a comparison of adder's power, performance, and area is conducted. According to the analysis of various architectures, the 32-bit CSA with RCPFA3 architecture performs the best in terms of power, delay and PDP for ASIC performance at the expense of increased area. In comparison to the traditional CSA and HCA adders, the suggested three-bit CSA_RCPFA3 enhances the energy (PDP) at a rate of 85.73% and 74.10%,
respectively

REFERANCES

[1] Jiang, H., Liu, L., Jonker, P.P., et al.: 'A high-performance and energyefficient FIR adaptive filter using approximate distributed arithmetic circuits', IEEE Trans. Circuits Syst. I, Regul. Pap., 2018, 66, (1), pp. 313–326

[2] Mittal, A., Nandi, A., Yadav, D.: 'Comparative study of 16-order FIR filter design using different multiplication techniques', IET Circuits Devices Syst., 2017, 11, (3), pp. 196–200

[3] Tang, Z., Zhang, J., Min, H.: 'A high-speed, programmable, CSD coefficient FIR filter', IEEE Trans. Consum. Electron., 2002, 48, (4), pp. 834–837

[4] Chen, K.H., Chiueh, T.D.: 'A low-power digit-based reconfigurable FIR filter', IEEE Trans Circuits Syst. II, Express Briefs, 2006, 53, (8), pp. 617– 621

[5] Mohanty, B.K., Patel, S.K.: 'Efficient very large-scale integration architecture for variable length block least mean square adaptive filter', IET Signal Process., 2015, 9, (8), pp. 605–610

[6] Meher, P.K.: 'Seamless pipelining of DSP circuits', Circuits Syst. Signal Process., 2016, 35, (4), pp. 1147–1162

[7] Peemen, M., Setio, A.A., Mesman, B., et al.: 'Memory centric accelerator design for convolutional neural networks'. Proc. IEEE 31st Int. Conf. on Computer Design (ICCD), Asheville, NC, USA, 2013, pp. 13–19

[8] Behrooz, P.: 'Computer arithmetic: algorithms and hardware designs' (Oxford University Press, USA, 2000)

[9] Cavanagh, J.J.F.: 'Digital computer arithmetic: design and implementation' (McGraw-Hill, USA, 1984)

[10] Koren, I.: 'Computer arithmetic algorithms' (AK Peters/CRC Press, USA, 2001)

[11] Wallace, C.S.: 'A suggestion for a fast multiplier', IEEE Trans. Electron. Comput., 1964, EC-13,(1), pp. 14–17

[12] Zimmermann, R.: 'Binary adder architectures for cell-based VLSI and their synthesis'. PhD thesis, Swiss Federal Institute Technology (ETH), Zurich, Switzerland, 1998

[13] Amin, A.: 'Area-efficient high-speed carry chain', Electron. Lett., 2007, 43, (23), pp. 1258–1260

[14] Efstathiou, C., Owda, Z., Tsiatouhas, Y.: 'New high-speed multioutput carry look-ahead adders', IEEE Trans. Circuits Syst. II, Express Briefs, 2013, 60, (10), pp. 667–671

[15] Kogge, P.M., Stone, H.S.: 'A parallel algorithm for the efficient solution of a general class of recurrence equations', IEEE Trans. Comput., 1973, 100, (8), pp. 786–793.