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APPLICATION OF DA-BASED LUT-BASED FIR FILTERS IN MIMO-OFDM BASED WIRELESS COMMUNICATION SYSTEMS

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Abstract
When it comes to MIMO-OFDM (Multiple-Input Multiple-Output Orthogonal Frequency Division Multiplexing) communication systems, digital signal processing (DSP) techniques are frequently utilized. A wide range of impairments can be mitigated through the application of these techniques, which are used to improve performance. Filtering, equalization, and channel estimation are just some of the functions that can be carried out with the help of finite impulse response (FIR) filters, which are utilized extensively in digital signal processing (DSP). Among the many factors that contribute to the reduction of inter-symbol interference (ISI) and inter-carrier interference (ICI) in MIMO-OFDM systems, these filters are among the most significant contributors. The channel, in addition to other impairments, is responsible for the occurrence of these interferences. A novel approach to the design of FIR filters is presented in this work. The approach makes use of Distribution Arithmetic based Lookup Tables (DA-LUTs) in conjunction with parallel registers. In order to enhance the throughput and efficiency of FIR filters, the focus of this work is on incorporating parallel registers into the DA-LUT architecture. As a result of the parallel registers' ability to perform computations and accumulate filter taps in parallel, the critical path delay is reduced, and higher filter operating frequencies are made possible. The proposed design methodology takes advantage of the benefits offered by DA, which makes it possible to effectively represent and manipulate numbers that have distributions that are not uniform within the population. DA-LUTs offer improved precision and reduced quantization errors in comparison to conventional uniform LUTs. This is accomplished by utilizing the inherent statistical properties of signal data during the processing of the signal. In addition, we will evaluate the performance of the DA-based LUT design in comparison to that of conventional FIR filters. The comparison takes into account a variety of criteria, including quantization errors, filter response accuracy, and hardware complexity, and it highlights the benefits of the approach that has been proposed.
Keywords— Multiple-Input Multiple Output, Orthogonal Frequency Division Multiplexing, Distribution Arithmetic, Lookup Tables.

1. Introduction

When it involves wireless communication structures that are primarily based on MIMO-OFDM, the utilization of FIR digital filters is an extremely important element. These filters are vital for a wide variety of features which are finished in the digital sign processor (DSP), along with signal filtering, equalization [1, and noise correction]. Nevertheless, achieving excessive-speed implementation of FIR filters even as simultaneously limiting electricity consumption has become a severe hassle. This is especially genuine whilst contemplating the accomplishments that have been made inside the field of VLSI generation [2] and the sizable software of virtual sign processors.

There had been some of distinctive attempts made to broaden specialized and bendy designs for the implementation of FIR filters on ASIC [3] and FPGA platforms [4]. The MIMO-OFDM-based communication systems where those designs are applicable [5] are particularly relevant. An extensive sort of problems served because the impetus for the development of those architectural designs. Systolic

designs, which can be characterized through simplicity, regularity, and modularity, become an attractive architectural paradigm for effectively enforcing computation-extensive DSP programs [6]. These designs provide the ability for high throughput thru the usage of strategies such as pipelining and parallel processing. Although there had been improvements, traditional architectures, that are closely depending on multipliers, have boundaries in terms of the amount of chip area to be had and the range of processing elements (PE) that can be covered [7]. As a end result of its excessive-throughput processing abilities, regularity, and price-powerful computing designs, the multiplier-less DA-based approach has received recognition as a means of addressing those constraints. When it involves FPGA implementation, this method is particularly promising as it uses the LUT structures that are inherent in FPGA logic [8].

When it involves MIMO-OFDM communique systems, FIR filters that have a limited impulse reaction are vital for efficient sign processing. Even though they're correct, the same old methods frequently face problems in terms of the quantity of area hired, the quantity of electricity consumed, and the processing speed. The findings of this look at present a novel approach that makes use of DA-LUTs in an effort to stay away from these limitations. [9] The proposed technique is constructed on the muse of DA, that's a mathematical framework that makes it easier to carry out calculations speedy with the aid of utilising chance distributions. Through the usage of DA-LUTs for arithmetic operations and the illustration of clear out coefficients as possibility distributions, the layout system for FIR filters may be simplified, which in the end results in improved performance in phrases of area performance, electricity consumption, and processing velocity [10]. A nuanced adjustment of precision tiers in DA-LUTs is made feasible with the aid of the adaptability of this method, which strikes a stability among performance and resource utilization.

The following is the organizational structure of the remaining parts of the article: A survey of the relevant literature, along with some objections, may be found in section 2. Within Section 3, a comprehensive study of the DA-LUT based FIR filter that has been developed is presented. The information on the proposed DA-LUT based FIR filter is included in Section 4, which provides the simulation information. At this point, the article is complete with section 5.

2. Literature Survey

Ganjikunta et al. [11] presented a DA architecture with the intention of using it for applications related to biomedical signal processing. It is possible for this architecture to carry out FIR filters in an efficient manner. Since this results in greater efficiency, it is preferable to use an approach that is based on LUTs when designing FIR filters. This is because this approach is more effective. An FIR filter was proposed to be implemented on the Xilinx Spartan3e FPGA environment. This filter was developed with the help of DA. The individuals who were responsible for carrying out this study were Magesh and his colleagues. With regard to the computation sharing multiplier (CSHM) that is currently being utilized, the CSHM-based FIR on DA that was suggested occupies less space in terms of FPGA slices and has a lower latency. This is in comparison to the CSHM that is currently being utilized. In order to achieve the best possible results while simultaneously generating a digital filter with an unlimited impulse response, Kaur et al. [13] developed a search algorithm that makes use of high-level synthesis and combines chimp and cuckoo in an original manner. This was done in order to achieve the best possible results. There are a total of 23 standard functions and three different kinds of infinite impulse response (IIR) models that have been used in the analysis of the effectiveness of the method that has been provided.

In order to ascertain the optimal filter coefficients for the LPFIR-WSOA filter, Karthick et al. [14] devised the water strider optimization approach. This was done in order to determine the optimal filter coefficients. Using the Virtex 6 and Virtex 7 target families, the LPFIR-WSOA filter that has been described has been implemented in FPGA in order to make it usable in real-time applications. This was accomplished by utilizing the Virtex 6 and Virtex 7 implementations. Odugu et al. [15] proposed a new block-based generic filter bank design that was utilized for a variety of two-dimensional symmetric FIR

filers. This design found application in the field. Putting into action the strategy that was suggested in order to achieve the objective of reducing the amount of space, storage memory, and power consumption that the filter bank requires is the goal that is being pursued.

3. Proposed Methodology

The proposed DA-LUT based FIR filter out, that is introduced for MIMO-OFDM applications, is subjected to a comprehensive evaluation on this section. The system architecture of the proposed method is depicted in Figure 1. This methodology makes use of parallel registers, FIR filter coefficients, and the DA-LUT so that it will attain high-pace and green filtering of input facts. Through the usage of distribution arithmetic for arithmetic operations, the DA-LUT is a critical component in the accomplishment of the intention of improving computational efficiency. The recursive nature of the filtering operation is ensured by using the feedback loop that extends from the filtered output to the accumulator. This feedback loop is an enormous contributor to the general effectiveness of the MIMO-OFDM-FIR clear out.

The technique is answerable for beginning the advent of the input data, that's generally known as x(n). The sign that wishes to be filtered inside the MIMO-OFDM-FIR device is represented by means of these input records. Next, the information this is being fed into parallel registers is subjected to parallelization as its miles being processed. By processing statistics in parallel, this parallelization makes it viable to process a couple of records streams at the identical time, which in turn improves the efficiency of the computation.

In addition, the coefficients of the FIR filter, which are represented by means of the symbol h(n), are initialized. The subsequent filtering operations depend on these coefficients, which play a sizeable element in defining the traits of the FIR filter out and are important for the filtering operations. Next, gift the DA-LUT, that's a critical factor of the technique that has been proposed. Through the storage of pre-calculated values associated with opportunity distributions linked to the FIR filter out coefficients, the DA-LUT makes it feasible to perform arithmetic operations in an effective manner. Through the usage of distribution mathematics, the computation system is simplified, which ends up in advantages in terms of both pace and the efficiency with which sources are applied.

The accumulator is in the end delivered into play at this factor. This element is accountable for amassing the results of the arithmetic operations that had been achieved with the DA-LUT. The output of the accumulator, which is denoted through the symbol y(n), is the output of the MIMO-OFDM-FIR device in any case filters had been applied. Concurrently, there's a remarks loop that connects the output y(n) to the accumulator through shift registers with the accumulator. A recursive system is created by way of this remarks loop, which ensures that the output contributes to subsequent iterations. This procedure allows the filter out to take into consideration previous outputs when generating the outcomes which might be currently obtained. It is important to notice that the recursive nature of FIR filtering is a fundamental feature.

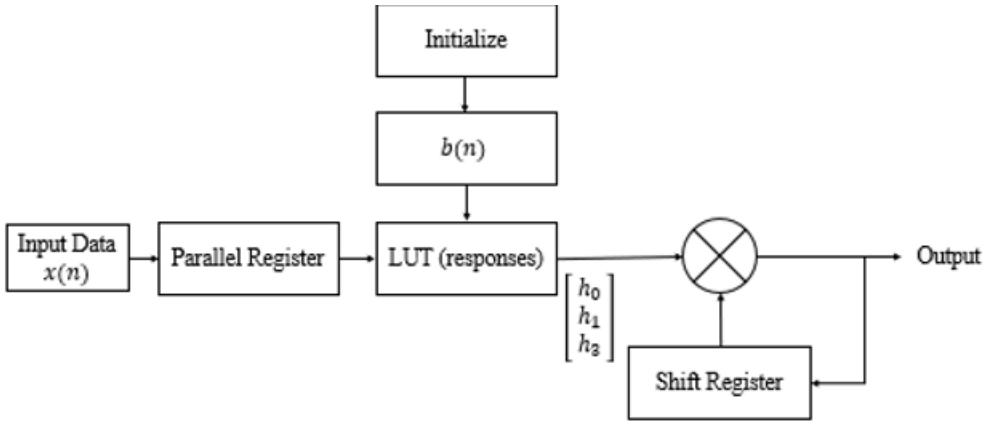

Fig. 1. Proposed DA-LUT based FIR filter block diagram.

A. Parallel Registers

The storing and retrieval of binary statistics in a parallel fashion is accomplished thru the utilization of digital circuits that are known as parallel registers. A wide variety of packages regularly employ them. Some examples of these packages include statistics buffering, information delivery, and facts synchronization, to call just a few of the programs that make use of them. As part of this comprehensive look at, we will check out the fundamentals of the way parallel registers perform, as well as the several bureaucracy, programs, benefits, and disadvantages of these registers.

A collection of turn-flops, commonly of the D-type, which are connected to one another to keep binary facts in a parallel fashion is referred to as a parallel sign up. The potential of every turn-flop is good enough for the storage of a parallel little bit of information. Parallel connections are made among the data inputs and facts outputs of the turn-flops. This allows the facts inputs to be received, and in a similar way, the records outputs of the turn-flops are related in parallel so that the records outputs can be delivered. Both eventualities involve the facts inputs and data outputs of the flip-flops being linked in parallel. This lets in for the records inputs and the information outputs to be received concurrently. To save statistics in a parallel check in, the data this is being input must first be applied simultaneously to the enter pins of each flip-flop this is contained within the register. Following the activation of a control sign, including a clock pulse, the information is secured onto the turn-flops so that you can get prepared for in addition processing. As a result of this, it is viable for the flip-flops to concurrently save all the bits that represent the records this is being acquired. Similarly, to retrieve the facts that has been saved within the parallel sign up, it's miles essential to retrieve the facts that has been saved in each turn-flop concurrently via connecting the output pins of the flip-flops collectively. This is done so one can retrieve the information. Following that, the information is without difficulty reachable in parallel layout thru the output pins of the register.

Parallel-In, Parallel-Out (PIPO) Register: This kind of parallel sign up lets in statistics to be loaded in parallel and study out in parallel on the identical time. It is also known as a parallel sign in. Since its enter and output pins are parallel, it could offer simultaneous data transmission. The Serial-In, Parallel-Out Register, additionally called the SIPO Register, is a register that reads facts in a sequential fashion and then writes it out in a parallel format. Even though it handiest has one information input pin, it has a huge wide variety of output ports which can produce parallel data. Parallel-In, Serial-Out (PISO) Register: The PISO sign up is responsible for receiving statistics that is furnished in parallel after which ultimately turning in those facts in a serial fashion. Additionally, it affords some of parallel enter ports in addition to an parallel serial output pin available. Universal Register: The ordinary sign up is a device that combines the competencies of all the exclusive kinds of registers right into a parallel system. Additionally, it allows for input and output operations to be accomplished in both parallel and serial formats, which offers flexibility inside the processing of facts.

B. DA-LUT

For all intents and purposes, a DA-LUT is nothing more than memory that stores values that have been precalculated in advance for the numerous possible combinations of input data. Because of this, the table can process the data in a timely and accurate manner. This table presents the DA-LUT operation table that has been proposed. Using this method, the DA-LUT is used to perform a preliminary calculation on all of the inputs and then store the results. The input of the filter is directed toward the DA-LUT, which is the one that is being addressed. When referring to a filter that has four inputs, the term "four tap" signifies not only the number of coefficients that the filter possesses, but also the number of inputs that the filter possesses in addition to the address bit for the DA-LUT. In other words, the term encompasses all of these aspects of the filter. The reason for this is that the phrase "four tap" simultaneously represents all of these things.

Table. 1. Third order DA-LUT performance table.

Address	Data
0000	0
0001	h_3
0010	h2
0011	h2 + h3
0100	h1
0101	h1 + h3
0111	h1 + h2 + h3
1000	h0
1001	h0 + h3
1010	h0 + h2
1011	h0 + h2 + h3
1100	h0 + h1
1101	h0 + h1 + h3
1110	h0 + h1+ h2
1111	h0 + h1 + h2 + h3

As a result of the inputs that it receives, each location generates a distinct output in response to those conditions. Valid inputs for this filter include values ranging from 0 (0000) to 15 (1111), which are listed in the range. When utilizing this method, it is not difficult to compute the result for each element of the input that is provided. For example, if the value that is being input is 1011, the output value will be 1.h0 plus 0; h1 plus 1; h2 plus 1; and h3 will equal h0 plus h2 plus 1.h3. If the value that is being input is 1111, the value that will be output will be h0 plus h1 plus h2 plus h3. When the value 0101 is used as the input, the value that is produced will be h1 plus h3. It is possible that the output value will be h0 plus h2 if the value that input is is 1010. A high-level input coefficient is incorporated into the system, as indicated by this term. It is not necessary for us to perform any kind of mathematical calculation to determine that there are sixteen outputs for every matching input.

C. Distributive Arithmetic

A bit serial procedure known as DA is used in the computation of FIR filter operations such as correlation, convolution, and inner products. These are all examples of DA. The relevance of DA lies in the fact that it can be mechanized with a high degree of efficiency. When the filter order in a simple DA implementation is raised, the LUT size also rises, which influences both the amount of space and the performance of the implementation. Using the LUT idea, both the performance and the size of the DA was improved. In this case, a signed data value of $(1, 1)$ is used rather of the binary data value of $(1, 0)$. The following expression describes the output of a FIR filter with a 'N' order: y(n). Let us have a look at the inner product of the two vectors d and x, which is given as

$$y = \sum_{k=1}^{K} d_k x_k \quad (1)$$

Here, d_k is a constant coefficient, x_k is the input signal, and K is the total number of words in the input. It is mathematically impossible for the value of the scaled binary integer x_k, which has digits that are the two's complement of one another and N bits, to be more than one. This number has digits that are the two's complement of one another. It is also possible to write x_k as:

$$x_k = -b_{k0} \sum_{n=1}^{N-1} b_{kn} 2^{-n} \quad (2)$$

$$x_k = \{b_{k0}, \dots \dots \dots \dots b_{k(N-1)}\} \quad (3)$$

Here, b_{kn} is the Nth bit of the x_k value that is being represented. The extended form of y was found by substituting equation (3) into equation (2), which results in the following:

$$y = \sum_{k=1}^{K} d_k [-b_{k0} + \sum_{k=1}^{K} d_k (-b_{k0})] \quad (4)$$

In mathematical notation, the expression for the inner product is often represented by the equation (3). If DA rearrange the way in which the totals are tallied, DA were able to arrive at the equation that is shown below at the end.

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$$y = \sum_{k=1}^{K}[\sum_{k=1}^{K} d_k b_{kn}]2^{-n} + \sum_{k=1}^{K} d_k(-b_{k0}) \quad (5)$$

In the form of x_k, let us write it out.

$$x_k = \frac{1}{2}[x_k - (-x_k)] \quad (6)$$

It is possible to describe the form of $-x_k$ that corresponds to the two's complement using the symbol.

$$-x_k = -\bar{b}_{k0} + \sum_{n=1}^{N-1} \bar{b}_{kn} 2^{-n} + 2^{-(N-1)} \quad (7)$$

By solving equation (6) using x_k and $-x_k$ as inputs:

$$x_k = \frac{1}{2}\left[-\left(b_{k0} - \bar{b}_{k0}\right) + \sum_{n=1}^{N-1}\left(b_{kn} - \bar{b}_{kn}\right) 2^{-n} - 2^{-(N-1)}\right] \quad (8)$$

For the sake of notational simplicity, let us assume.

$$S_{kn}\left\{ \begin{matrix} b_{kn} - \bar{b}_{kn}, n \neq 0 \\ \left(b_{kn} - \bar{b}_{kn}\right), n \neq 0 \end{matrix} \right\} \quad (9)$$

Here,

$$P(b_n) = \sum_{k=1}^{K} \frac{d_k}{2} S_{kn} \quad (10)$$

$$P(0) = -\sum_{k=1}^{K} \frac{d_k}{2} \quad (11)$$

Here, $P(0)$ is the only word-initial condition register, while $P(b_n)$ may take on a total of $2^{(k-1)}$ different values depending on the context. A word-initial condition register is denoted by the symbol "$P(0)$.". Because of this, the total amount of LUT that was used in DA has been reduced to merely 2^{k-1} rather of the entire 2^k.

4. Results and Discussion

This part of the article provides a comprehensive simulation analysis of the DA-LUT based FIR filter that has been proposed. Simulations are carried out in this location with the assistance of the Xilinx-VIVADO software tool. The result of the simulation is depicted in Figure 2, which includes the sign, clk, and rst as primary inputs, x as data input, and h0, h1, h2, and h3 as impulse coefficient inputs of the DA-LUT. Furthermore, the data out output is the final output of the FIR filter that is based on DA-LUT.

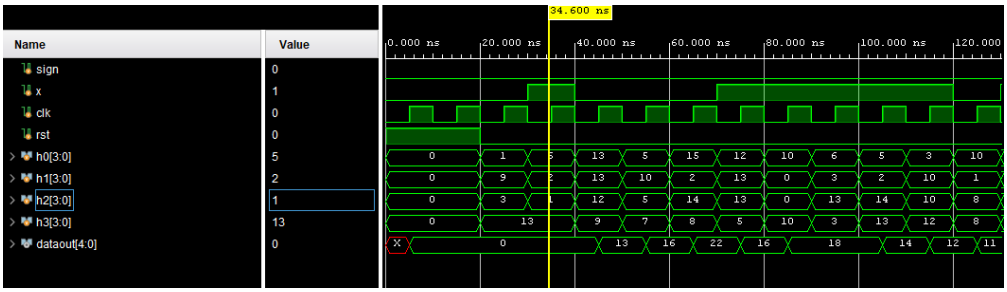

Fig. 2. Simulation output

The resource utilization on the FPGA for the proposed DA-LUT-FIR filter is visually represented in Figure 3, which provides a comprehensive snapshot of the situation. Programable logic blocks, also known as LUTs, are used to implement combinational logic functions. Out of the 78,600 LUTs that are available, 61 are currently being utilized. The number of Flip-Flops (FFs), which are used to store binary information, is calculated to be twelve out of the total of 157,200 that are available. Out of the total of 250 available blocks, 25 are used by input/output blocks (IoBs), which are responsible for interacting with external devices. In addition, the figure illustrates the utilization of Phase-Locked Loop (BUFG) components, which includes the utilization of one out of every 32 components. These values, when taken together, provide a quantitative measure of the proposed DA-LUT-FIR filter's effective utilization of FPGA resources.

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Resource	Utilization	Available	Utilization...
LUT	61	78600	0.08
FF	12	157200	0.01
IO	25	250	10.00
BUFG	1	32	3.13

Fig. 3. Design summary.

Figure 4 provides a precis of the setup time, which sheds light at the timing traits of the machine this is being proposed. There is a total put off 6.139 nanoseconds, which includes the time this is required for logic operations (3.192 nanoseconds) and the internet put off (2.947 nanoseconds). The time it takes for indicators to become stable earlier than they are sampled is known as the setup time, and those figures offer crucial insights into the temporal overall performance of the DA-LUT-FIR filter.

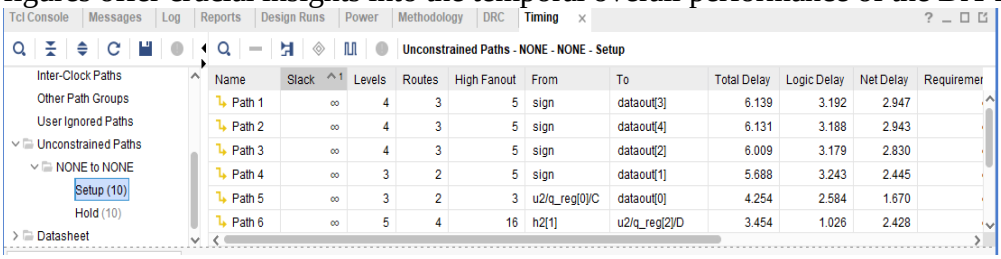

Fig. 4. Setup Time summary.

In order to make sure that the sign stays strong, the hold time is an essential parameter, and Figure 5 provides a detailed breakdown of this parameter. There are two additives that make up the full postpone of 0.313ns: the good judgment put off (0.128ns) and the net put off (0.185ns). The term "preserve time" refers to the minimum amount of time that a sign need to stay solid after being sampled, and the values that indicate this are taken into consideration while figuring out the temporal robustness of the system.

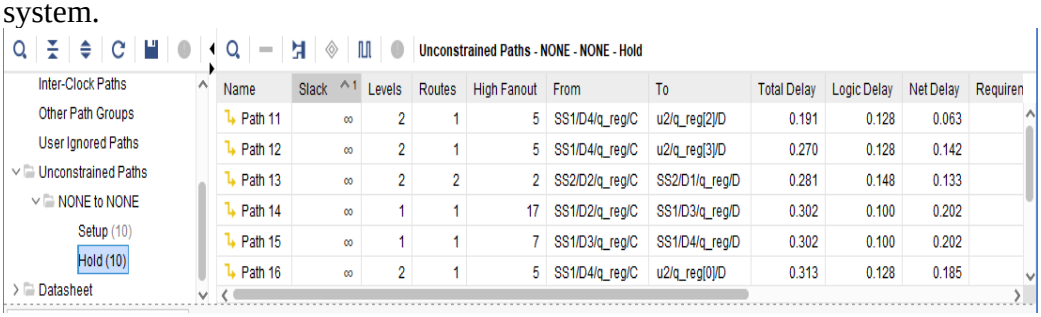

Fig. 5. Hold Time summary.

The proposed DA-LUT-FIR filter out is displayed in Figure 6, which affords a comprehensive evaluation of the electricity consumption of the filter out. Dynamic and static components are the two classes which can be used to categorise the power values. In order to don't forget the variations in sign interest, dynamic strength is in addition broken down into three classes: sign power (0.430uw), good judgment power (0.408uw), and IoB strength (4.268uw). Additionally, the static energy component is furnished in its personal proper (0.115uw). It has been decided that the total dynamic energy is five.106 uw, and while that is added to the static power, the total strength consumption for the device is five.22 uw. These metrics offer valuable insights into the strength efficiency and energy traits of the DA-LUT-FIR clear out that has been proposed, which facilitates in determining whether or not or no longer it is appropriate for practical programs.

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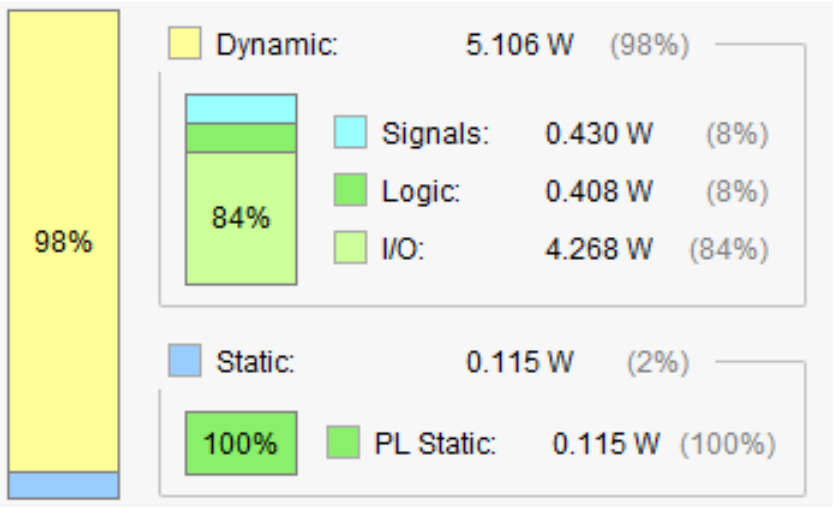

Fig. 6. Power summary

The area utilization was compared between the existing filter and the proposed filter in Table 2, which can be found below. The number of LUTs has been decreased by approximately 29.07%, which indicates that the implementation of combinational logic functions has become more efficient. Furthermore, there is a significant reduction in FFs, which is approximately 65.71%, which suggests that the storage of binary information has been simplified overall. IoBs also experience a significant decrease of approximately 55.36%, which indicates that their interfacing with external devices has improved. Furthermore, the size of the BUFG components has been decreased by approximately 75%.

Table. 2. Area performance comparison.

Resource	Existing Filter	Proposed Filter
LUTs	86	61
FFs	35	12
IoBs	56	25
BUFG	4	1

5. Conclusion

The motive of this study is to investigate the optimization of FIR filters in MIMO-OFDM communique structures. Our technique, which makes use of DA-LUTs with parallel registers, is targeted on improving the efficiency and throughput of FIR filters, which are vital components in decreasing interference problems inside these structures. As a end result of the incorporation of parallel registers, concurrent computation and accumulation of filter taps are made less difficult. This results in a discount in the important route delay and makes it possible to operate FIR filters at better frequencies. The technique that has been proposed makes use of DA, which is a way that allows the effective representation and manipulation of numbers that have distributions that are not uniform. The inherent statistical houses of sign data can be exploited to achieve more suitable precision and reduce quantization mistakes while in comparison to traditional LUTs. This function is specifically useful in sign facts as it lets in for the utilization of these homes. The results of our research show that the DA-LUT design is advanced to the conventional FIR filters. This is tested via a complete performance contrast. A wide variety of things, along with quantization errors, filter out response accuracy, and hardware complexity, are covered in the evaluation criteria. The findings highlight the benefits of our approach, which makes a full-size contribution to the optimization of MIMO-OFDM structures by means of enhancing the effectiveness and precision of FIR filters thru the software of present-day digital sign processing techniques.

References

[1] Di Meo, Gennaro, et al. "A Novel Low-Power High-Precision Implementation for Sign–Magnitude DLMS Adaptive Filters." Electronics 11.7 (2022): 1007.
[2] Shrivastava, Prabhat Chandra, et al. "An Efficient Block-Based Architecture for Reconfigurable FIR Filter Using Partial-Product Method." Circuits, Systems, and Signal Processing 41.4 (2022): 2173-2187.
[3] Thamizharasan, V., and N. Kasthuri. "FPGA implementation of high performance digital FIR filter design using a hybrid adder and multiplier." International Journal of Electronics (2022): 1-21.
[4] Kumar, Gundugonti Kishore, et al. "Area-, Power-, and Delay-Optimized 2D FIR Filter Architecture for Image Processing Applications." Circuits, Systems, and Signal Processing 42.2 (2023): 780-800.
[5] Ezilarasan, M. R., J. Britto Pari, and Man-Fai Leung. "Reconfigurable Architecture for Noise Cancellation in Acoustic Environment Using Single Multiply Accumulate Adaline Filter." Electronics 12.4 (2023): 810.
[6] Sharada, K. A., et al. "High ECG diagnosis rate using novel machine learning techniques with Distributed Arithmetic (DA) based gated recurrent units." Microprocessors and Microsystems 98 (2023): 104796.
[7] Lakshmi, Vijaya, Vikramkumar Pudi, and John Reuben. "Inner product computation in-Memory using distributed arithmetic." IEEE Transactions on Circuits and Systems I: Regular Papers 69.11 (2022): 4546-4557.
[8] Diouri, Omar, et al. "Comparison study of hardware architectures performance between FPGA and DSP processors for implementing digital signal processing algorithms: Application of FIR digital filter." Results in Engineering 16 (2022): 100639.
[9] Vijetha, K., and Rajendra Naik. "Low power low area VLSI implementation of adaptive FIR filter using DA for decision feed back equalizer." Microprocessors and Microsystems 93 (2022): 104577.
[10] Wang, Xingyang, and Yutong Zhu. "Intelligent Art Design Management Based on Wireless Communication Microprocessor and Mobile Internet." Wireless Communications and Mobile Computing 2022 (2022).
[11] Ganjikunta, Ganesh Kumar, Mahaboob Basha Mohammed, and Inayatullah Khan Sibghatullah. "Energy Efficient FIR Filter Design Using Distributed Arithmetic." Journal of Shanghai Jiaotong University (Science) (2022): 1-5.
[12] Magesh, V., and N. Duraipandian. "Implementation of Programmable Finite Impulse Response Filter Using Modified Computation Sharing Multiplier for Hearing Aids." Wireless Personal Communications 129.1 (2023): 255-270.
[13] Kaur, Mandeep, Ranjit Kaur, and Narinder Singh. "A novel hybrid of chimp with cuckoo search algorithm for the optimal designing of digital infinite impulse response filter using high-level synthesis." Soft Computing (2022): 1-25.
[14] Karthick, R., et al. "Design and analysis of linear phase finite impulse response filter using water strider optimization algorithm in FPGA." Circuits, Systems, and Signal Processing 41.9 (2022): 5254-5282.
[15] Odugu, Venkata Krishna, C. Venkata Narasimhulu, and K. Satya Prasad. "A novel filter-bank architecture of 2D-FIR symmetry filters using LUT based multipliers." Integration 84 (2022): 12-25.