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FULLY AUTOMATED TRAFFIC LIGHT CONTROLLER SYSTEMFOR A FOUR- WAY INTERSECTION USING VERILOG

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ABSTRACT:
Traffic lights are placed in roads to control the flow of traffic and to prevent accidents. This paper proposes a Moore machine based fully automated and efficient traffic light controller system for four-way intersection. The system is designed on Xilinx Artix-7 xc7a100tcsg324-1 FPGA using Xilinx Vivado and Verilog Hardware Description Language (VHDL). The designed system runs up to a maximum operating frequency of 10 MHz.

Keywords—
Field Programmable Gate Array, Finite State Machine, Hardware Description Language, Light Emitting Diode, Verilog.

INTRODUCTION

Traffic congestion is one of the predominant problems prevailing in cities and towns. In T-intersection and four-way intersection, the probabilities of accidents are slightly higher. So, to ensure smooth flow of traffic and to avoid road accidents, traffic light systems are used. The proposed traffic light controller system is designed for four-way intersection roads. In this system, the waiting time of vehicles at the intersection is reduced by a great extent. Microcontroller and Microprocessor based traffic light systems are already present. But the disadvantage associated with these systems is that, they work on fixed time, and doesn't have flexibility.

So, this paper concentrates on developing a reconfigurable traffic light controller system, which works on Field Programmable Gate Array (FPGA) as it doesn't have a fixed hardware structureand can be reprogrammed by using Hardware Description Language (HDL). Verilog is chosen for modelling the traffic light controller system, as usage of Verilog HDL allows defining the specifications of the parameters used in the design of the system. Also, Verilog HDL is one of the commonly used HDLs as it has simple syntax and it resembles software programming languages to some extent. FPGA boards have many input switches and output Light Emitting Diodes (LEDs) in it,which make it suitable for the design of traffic light controller systems.

FPGAs are used for designing prototypes for many electronic applications. Another advantage of FPGA is that, it makes the whole system more efficient. The FPGA chosen here is Artix-7, which is a product of Xilinx, a semiconductor manufacturing company. Artix-7 is preferred as it is cost efficient and for its high performance. It is used in systems so as to have optimum power consumption. There are different types of traffic control systems which are put forth by researchers for different real time situations. A traffic light controller was designed using Verilog HDL considering two roads and for a T-junction.

A system for four-way intersection was implemented using two signals, red and green. Another system makes use of three signals, red, yellow and green to regulate the traffic. But the drawback of

these systems for four-way intersection was that they don't allow the maximum possible movement of vehicles across the intersection. Vehicles from few roads are made to wait at the intersection unnecessarily as allowing them doesn't disturb the moving vehicles. The proposed system makes sure that this drawback is removed to allow the maximum transportation of vehicles across the intersection and to prevent the unnecessary waiting time ofthe motorists.

Moore model of Finite State Machine (FSM) is used to design the traffic light controller system as the output of the system (traffic light signals) depends only upon the current state of the system. This feature makes the system fully automated. The system considers the four roads to have equal traffic and makes use of the Binary encoding scheme. Compared to other works, the proposed system is more efficient by making use of minimal number of states which are necessary enough to allow the maximum transportation of vehicles across the intersection. The reduction in number of states also helps in achieving minimal power consumption.

The traffic controller system also makes use of the maximum possible number of safe states. Before the stoppage of traffic across each direction, yellow signal is displayed in the corresponding displays which indicate that the flow of traffic will be stopped in few seconds. The states containing yellow signals act as safe states and prevent the possibility of accidents. A Simulation based system is designed and the same is done using Xilinx Vivado. Complete information of the system designed is obtained using various facilities present in this software like timing report, utilization report, power report, etc.

LITERATURE SURVEY

[1] Shabarinath B B and Swetha Reddy K (2017) "Timing and Synchronization for explicit FSM based Traffic Light Controller", IEEE 7th International Advance Computing Conference.

Traffic light control unit can be designed as a synchronous sequential machine with finite number of states. Explicit finite state model is used to design the necessary coding for control systemusing Verilog HDL. The machine is modelled with only six states and these states are chosen based on the traffic control algorithm. In each state necessary delay is provided and for that particular delaythe necessary traffic lights are set ON and OFF.

For illustration just only two roads are chosen and control algorithm controls the traffic lights of that roads. This paper proposes a flexible framework which provides a delay in particular state using clock divider, also discusses the issue of modelling the state machine in a synthesis friendly manner.

[2] Boon Kiat Koay and Maryam Mohd. Isa (2009) "Traffic Light System Design on FPGA", Proceedings of 2009 IEEE Student Conference on Research and Development (SCOReD 2009), 16-18 Nov. 2009, UPM Serdang, Malaysia.

This paper proposed a design of a modern FPGA-based Traffic Light Control (TLC) System to manage the road traffic. The approach is by controlling the access to areas shared among multiple intersections and allocating effective time between various users; during peak and off-peak hours. Theimplementation is based on real location in a city in Malaysia where the existing traffic light controlleris a basic fixed-time method.

This method is inefficient and almost always leads to traffic congestion during peak hours while drivers are given unnecessary waiting time during off-peak hours. The proposed design is a more universal and intelligent approach to the situation and has been implemented using FPGA.

[3] Venkata Kishore S (2017) "FPGA based Traffic Light Controller", International Conference on Trends in Electronics (ICEI).

The main purpose of the traffic light control system is to control the congestion of vehicles atthe junctions and also for safer pedestrian crossing. There have been many technologies used for implementing a traffic light controller all over the world. India being oneof the densely populated countries, upgrading to a new control system and imposing it all overis a tedious process.

This paper proposes the reconfigurable Traffic Light controller which can display the time ofwaiting in all the directions. It has been observed that the designed traffic light controller is working up to a

maximum operating frequency of about 300 MHz. The coding has been done using the Verilog Hardware Descriptive Language.

[4] D.Bhavana, D.Ravi Tej, Priyanshi Jain, G.Mounika, R.Mohini, Bhavana (2015)"Traffic Light Controller Using Fpga", International Journal of Engineering Research and Applications (IJERA).

The paper concentrates on developing a traffic light controller system for a four-way intersection. Each road has three light displays corresponding to the flow of traffic towards the other three roads. Hence there are twelve light displays in total at the intersection. By using common control logic, the system is designed in such a way that, certain light displays operate in the same manner. This simplifies the design with ten light displays.

Each of these light displays have the provision to show red, green and yellow signals. The redsignal specifies to stop, the green signal allows the flow of traffic and the yellow signal specifies thatthe flow of traffic will be stopped in few seconds. The proposed system helps top revent vehicle collisions at the intersection by use of 'safe' states. The red, yellow and green signals of each of the light displays are modeled as individual output LEDs.

Existing Method:

In existing method, there is separate controller for traffic light and counting.

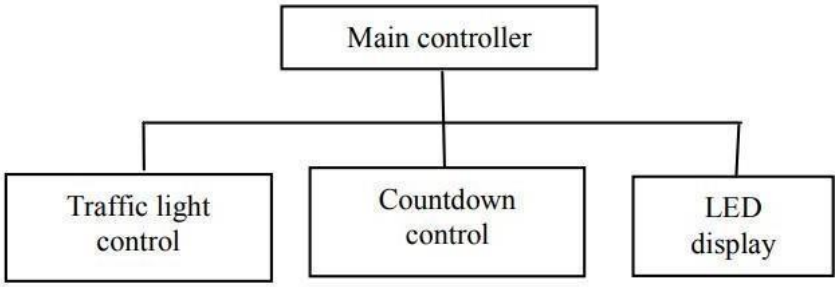

Fig1: Existing method

PROPOSED METHOD

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The red, yellow and green signals of each of the light displays are modeled as individual output LEDs. So a total of thirty output LEDs are used. A state diagram and a state table are constructedbased upon the simplified logic to model a finite state machine for the proposed traffic light controllersystem.

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Direction name	Corresponding movement of vehicles at the intersection
D0	
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	
D9	

Fig2: Directional Representation

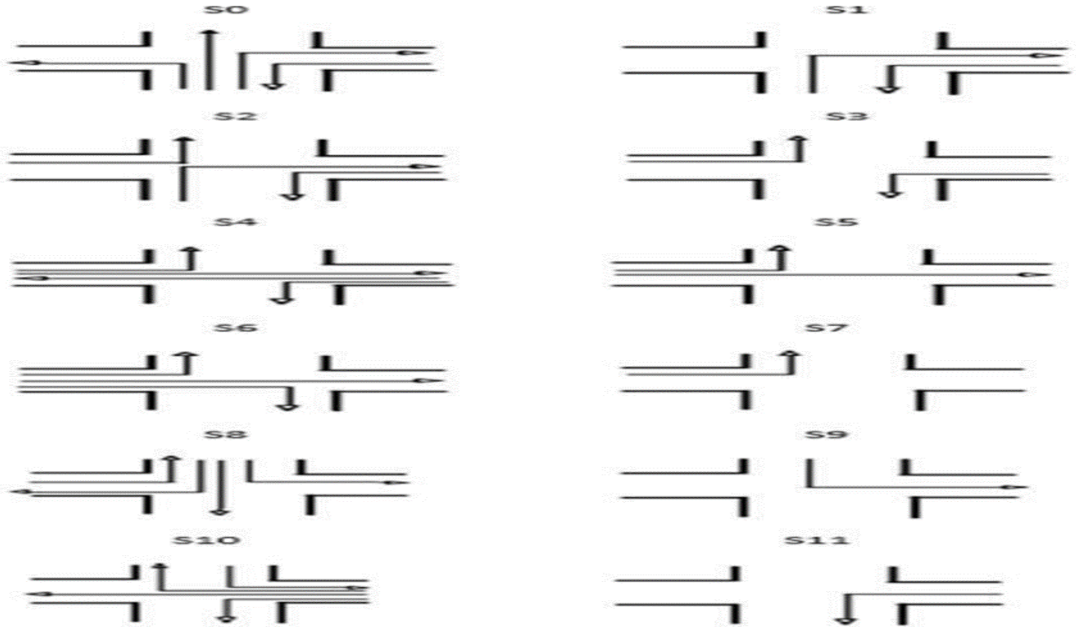

Fig3: Representation of states

State	Traffic signal status for each direction									
	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
S0	001	100	100	100	001	100	100	001	100	100
S1	010	100	100	100	001	100	100	001	100	100
S2	100	100	100	100	001	001	100	001	100	100
S3	100	100	100	100	010	001	100	001	100	100
S4	100	100	100	001	100	001	100	001	001	100
S5	100	100	100	010	100	001	100	010	001	100
S6	100	001	100	100	100	001	100	100	001	100
S7	100	010	100	100	100	001	100	100	010	100
S8	100	100	001	100	100	001	001	100	100	100
S9	100	100	010	100	100	010	001	100	100	100
S10	100	100	100	001	100	100	001	001	100	001
S11	100	100	100	010	100	100	010	001	100	010

Fig 4: State Transition Representation

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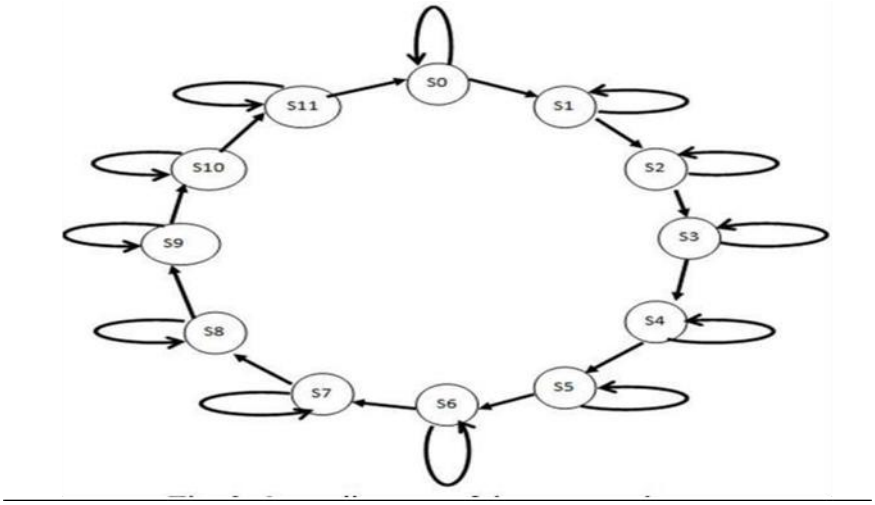

Fig 5: Direction State output Relation

Results:

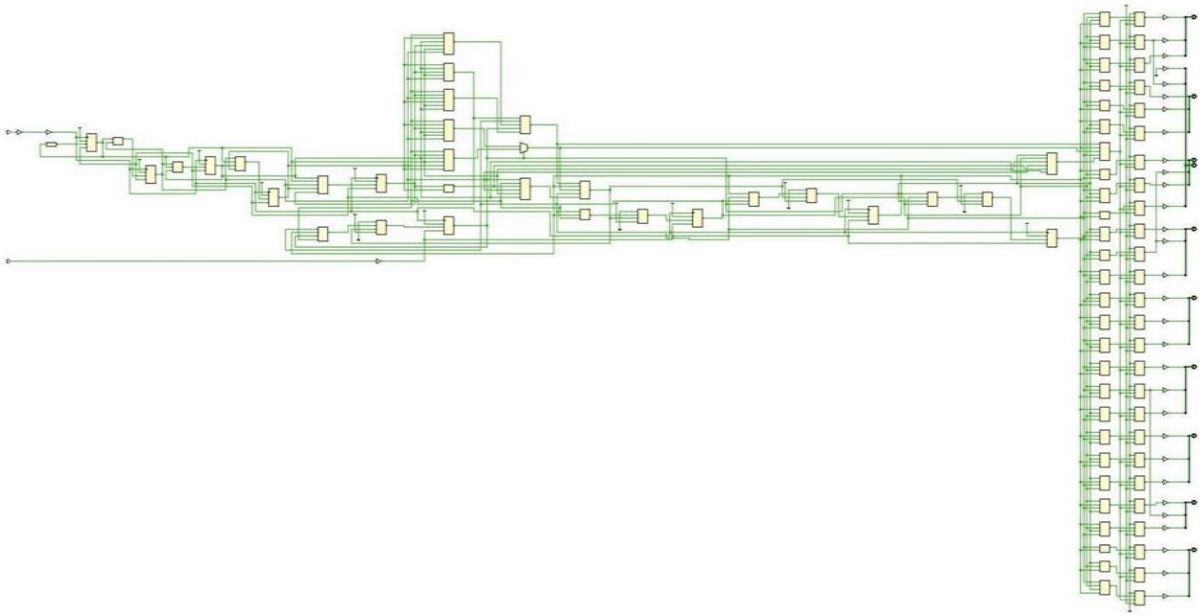

Fig6: RTL Schematic

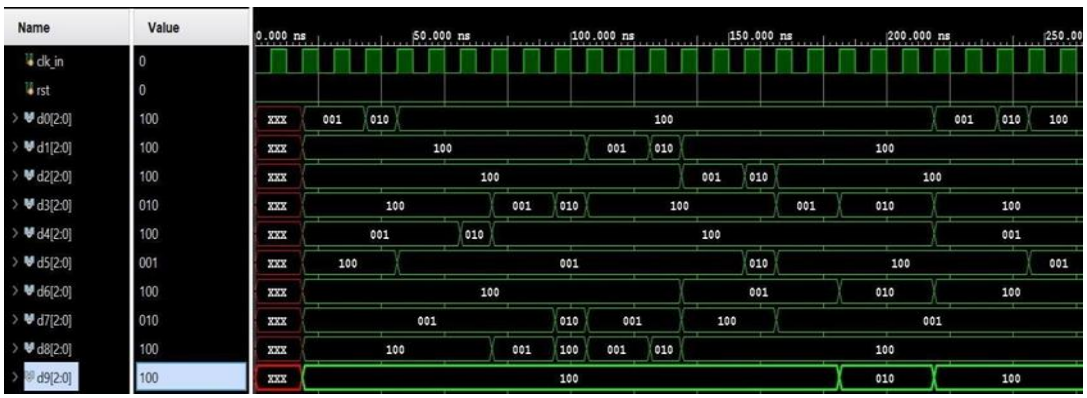

Fig7: Simulation results

Name	Slice LUTs (134600)	Slice Registers (269200)	F7 Muxes (67300)	Bonded IOB (400)	BUFGCTRL (32)
fsm_1	28	39	1	32	1

Table1: Area Analysis

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	2	2	1	d0_reg[0]/G	d0[0]	3.505	2.860	0.646
Path 2	∞	2	2	1	d0_reg[1]/G	d0[1]	3.505	2.860	0.646
Path 3	∞	2	2	1	d0_reg[2]/G	d0[2]	3.505	2.860	0.646
Path 4	∞	2	2	1	d1_reg[0]/G	d1[0]	3.505	2.860	0.646
Path 5	∞	2	2	2	d1_reg[1]/G	d1[1]	3.505	2.860	0.646
Path 6	∞	2	2	1	d1_reg[2]/G	d1[2]	3.505	2.860	0.646
Path 7	∞	2	2	1	d2_reg[0]/G	d2[0]	3.505	2.860	0.646
Path 8	∞	2	2	2	d2_reg[1]/G	d2[1]	3.505	2.860	0.646
Path 9	∞	2	2	1	d2_reg[2]/G	d2[2]	3.505	2.860	0.646
Path 10	∞	2	2	1	d3_reg[0]/G	d3[0]	3.505	2.860	0.646

Table2: Delay Analysis

CONCLUSION

The traffic light controller system designed is well suited to regulate traffic at four- way intersection. The system is designed in Artix-7 FPGA so as to utilize its advantage of efficient power consumption. Verilog HDL is used for programming purpose because if the user wishes to make any changes in the system, it is possible to apply the required changes easily through Verilog HDL code. One of the advantages of this system is its 'safe state' feature implemented in every odd state, which plays a major role in preventing vehicle collisions.

As a future scope, cameras and sensors can be integrated to the designed system so that when the traffic controller system sees an ambulance, it can automatically divert the traffic accordingly so as to ensure that there is no obstacle and the way for the ambulance is clear.

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