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A SURVEY AND NOVEL APPROACH USING FAST FOURIER TRANSFORM ARCHITECTURES

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ABSTRACT: In this paper, a variety of available FFT algorithms are presented and then different architectures are outlined by exploring the techniques and algorithms involved in each of the architectures. The widely adopted architectures and trends in architectural modification to reduce power consumption and area and to achieve high throughput are discussed this concept proposes an efficient memory-based radix-2 FFT architecture, which greatly improves the memory based FFT by reducing area requirement, while maintaining a simple address generator.

These architectures were designed to maximize hardware utilization by employing techniques such as folded transforms and register minimization. The goal was to reduce the number of adders while ensuring efficient computation that are serial and interrelated architectures.

The evaluation criteria included throughput, resource utilization, and energy consumption. Low-Energy Real FFT Architectures are the three architectures studied were

SingleProcessingElement(SPE): Astraightforward approach.

Pipelined:Leveragingpipeliningtechniquesforimprovedefficiency.

InPlace: Optimizingmemoryaccesspatterns.Thegoalwastostrikeabalancebetween performance and energy efficiency.

In summary, researchers continue to explore innovative ways to optimize hardware utilizationforreal-valuedFFTs.Theseeffortscontributetoefficientsignalprocessingsystems, enabling applications in fields such as communications, audio processing, and medical diagnostics.

INTRODUCTION

Fast Fourier Transform (FFT) algorithm is widely used in many signal processing and communication systems. Due to its intensive computational requirements, it occupies large area and consumes high power if implemented in hardware. Efficient algorithms are developed to improve its architecture.TheFastFouriertransform(FFT)isoneofthemostimportantalgorithmsinthefieldofdigital signal processing. Itis used to calculatethe discreteFouriertransform (DFT)efficiently. Inorder to meet the high performance and real-time requirements of modern applications, hardware designers have always tried to implement efficient architectures for the computation of the FFT.

In this context, pipelined hardware architectures are widely used, because they provide high throughputs and low latencies suitable for real time, as well as a reasonably low area and power consumption.There are two main types of pipelined architectures: feedback (FB) and feedforward (FF). On the one hand, feedback architectures are characterized by their feedback loops, i.e., some outputsofthebutterfliesarefedbacktothememoriesatthesamestage.Feedbackarchitecturescan be divided into single-path delay feedback (SDF), which process a continuous flow of one sample per clock cycle, and multi-path delay feedback (MDF) or parallel feedback, which process several samples in parallel. On the other hand, feedforward architectures, also known as multi-path delay commutator (MDC) , do not have feedback loops and each stage passes the processed data to the next stage.

These architectures can also process several samples in parallel. In current real-time applications, the FFT has to be calculated at very high throughput rates, even in the

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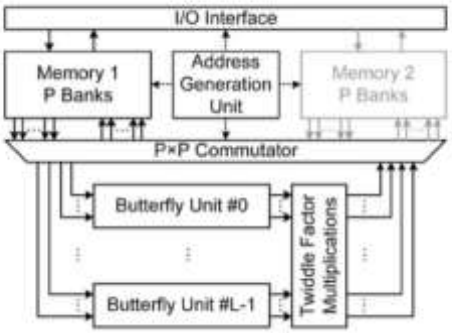
range of Gigasamples per second. These high-performance requirements appear in applications such as orthogonal frequency division multiplexing (OFDM),and ultra wideband (UWB) . In this context two main challenges can be distinguished. The first one is to calculate the FFT of multiple independent data sequences. In this case, all the FFT processors can share the rotation memory in order to reduce the hardware . Designs that manage a variable number of sequences can also be obtained.Thesecondchallengeistocal culatetheFFTwhenseveralsamplesof thesamesequence are received in parallel. This must be done when the required throughput is higher than the clock frequency of the device. In this case it is necessary to resort to FFT architectures that can manage several samples in parallel.

As a result, parallel feedback architectures, which had not been considered for several decades, have become very popular in the last few years. Conversely, not very much attention has been paid to feedforward (MDC) architectures. This paradoxical fact, however, has a simple explanation. Originally,SDF and MDCarchitectures wereproposed forradix-2 and radix-4. Some yearslater,radix-waspresentedfortheSDFFFTasanimprovementonradix-2andradix-4.

EXISTING ARCHITECTURE



Multiple-PE,memory-basedFFTprocessor

The conflict-free address scheme for SPPFFTs presented by Tsai and Lin [12] is illustrated onlyfor2*n*-pointFFTs.Wecanextend themethodtoarbitrary-lengthsingle-power *rn*-pointFFTs by replacing the XOR operations in (8) and (9) with *r*-modulo additions.Assume that the $N = rm$- point FFT employs a mixed radix with the maximum radix-r q MDC units. The parallelism of the MDC PE is $P = r$ p, and P must divide $rm-q$, the number of butterflies at each stage.As a result, formation (1) can be transformed into

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$$\frac{N}{r \cdot r^{p}} \cdot \lceil \log_{r^q} r^{m} \rceil \leq N \rightarrow \left\lceil \frac{m}{q} \right\rceil \leq r^{p+1}.$$

However,asthethroughputofSPPFFTsisassociatedwiththePEnumberclosely,itiscritical to explore the relationship between the number of constraint sets and the applied algorithm under different cases.

*1)OnlyIncreasingthePEParallelismortheButterflyRadix:*Ifweonlyincreasetheparallelism of the PE *P*, while keeping the butterfly radix as the simplest radix-*r*, then *q* = 1,and (10) will become $m \leq r\,p+1$. For any stage *s*, the *r* parallel data indices are only different in the (*m*−*s*−1)th digit. Forthe *m*-level forwardaddress representation, thereare *m*differentconstraint sets and vice versaAs a result, there arein total *m* disjoint constraint sets forthe radix-*r* FFT.

LITERATURE SURVEY

The references given in the following are related with the DFT and FFT based control algorithms in power quality issues. A method for the calculation of bus voltage transients in an electricpowersystemispresented(Heydt,1989).Theessenceofthemethodistheﬁnitetransform of Ohm's law. The fast Fourier transform is used in order to give computational efficiency.

Twoapproximationsarefoundforthecalculationofthistransferimpedanceandoneofthese isfoundtobeapplicabletothecitedproblem.Examplesareusedtoillustratethecalculationofbus voltage transients and harmonic content. The Gibbs phenomenon appears in a discrete Fourier transform due to incomplete periodic, the waveform has not reached a full cycle within its period. Data flipping furnishes a complete periodic cycle to the waveform and thus suppresses the Gibbs phenomenon.

This facilitates the design of a digital filter using fast Fourier transform without windowing. Thefilterdoeslow-pass,band-pass,high-pass,band-stop,notchorsingle-frequency-passsimplyby manipulating the band limits. The filter can be affected by spectral resolution and the slope discontinuity at the end data points. The reduction of such effects and an alternative design are discussed(Pan,1993).Theevaluation ofDFTspectrausuallyyieldsmoredeta

iledinformationthan evaluation in the time domain is presented (Breitenbach, 1999). The evaluation of time-discrete spectra, hampered by leakage, which occurs if a non-integral number of periods, is present in the sampled data set. Minimization of spectral leakage is an important prerequisite for spectrum analysis. The use of non-rectangular time domain windowing functions offers some improvement butalsoinvitesunwantedside-effects.Spectralleakagecanbeavoidedentirelybyensuringthat an integer number of periods falls into the sampling time (e.g. by the use of coherent sampling).

The application of the windowed fast Fourier transform to electric power quality assessment is presented (Heydt et al., 1999). The windowed FFT is a time windowed version of the discretetimeFouriertransform.Thewindowwidthmaybeadjustedandshiftedtoscanthroughlarge volumesofpowerqualitydata.Narrowwindowwidthsare usedfor detailedanalysesandwide window widths are used to move rapidly across archived power quality data measurements.

harmonicanalysisisproposedforthefrequencyandphasorestimatingalgorithm(Yangetal.,2005).

The major components of the method are a frequency and phasor estimating algorithm, a finite-impulse-response comb filter and a correction factor. It also combines other methods to enhance our performance, such as discrete Fourier transform and least square error method. To verifyproposedmethod,itcomparesFFT.

RELATED WORK

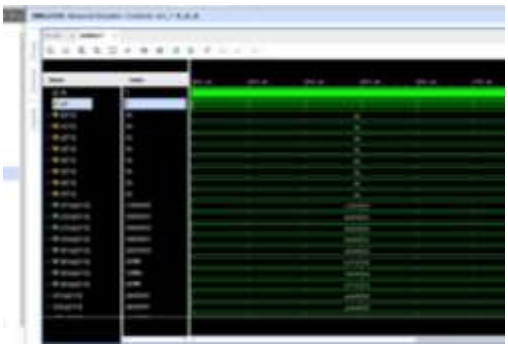
Modified Booth Algorithm Encoder

This modified booth multiplier is used to perform high-speed multiplications using modified booth algorithm.This modified booth multiplier's computation timeand thelogarithm of theword lengthofoperandsareproportionaltoeachother.Wecanreducehalfthenumberofpartialproduct. Radix-4 booth algorithm used here increases the speed of multiplier and reduces the area of multiplier circuit. In this algorithm, every second column is taken and multiplied by 0 or +1 or +2 or-1or-2insteadofmultiplyingwith0or1after

shiftingandaddingofeverycolumnof thebooth multiplier.Thus,halfofthepartialproductcanbereducedusingthisboothalgorithm.Basedonthe multiplier bits, the process of encoding the multiplicand is performed by radix-4 booth encoder.

Theoverlappingisusedforcomparingthreebitsatatime.Thisgroupingisstartedfromleast significant bit (LSB),in which only two bits of the booth multiplier are used by the first block and a zero is assumed as third bit as shown in the figure.

SAMPLE RESULTS



The FFT is a crucial algorithm in digital signal processing. It allows us to convert continuous signals from the time domain into the frequency domain. For discrete data (such as those encountered in digital systems), we use the Discrete Fourier Transform (DFT) instead. The DFT transforms a finite sequence of equally spaced samples into a corresponding frequency domain representation. FFT is implemented can be decimation in time and decimation in frequencydomain.thesetwodomains areexecutedatsametime.intheabove resultclkissetas1 and 0.set value is always 1.here ‘s’values are DIF and ‘d’values are DIT. Hardware chip performance analysis of different FFT architecture.

Building Blocks:

- **Butterflies**:TheseperformthecorecomputationsinntheFFT.Theycombinetwoinput values and produce two output values.
- **Rotators**:Responsibleformultiplyinginputvaluesbytwiddle factors.

ShufflingCircuits:HandledatareorderingduringtheFFTprocess.

CONCLUSION

In this project We present memory-based FFT implementations with generalized efficient conflict-free address schemes.. For both SPP and NSPP FFTs, high-radix algorithm and parallel-processing technique can be used to increase the throughput. And the address scheme for FFTs applied with PFA is explored. Moreover, a decomposition method, named HRSB, is designed to suit the high-radixalgorithm.Theproposednewstructuresignificantlyreducesthememorysize,whilemaintains the same speed performance, compared with its predecessor.

FUTUREENHANCEMENT

The future works will be enhancing the proposed architecture for variable length FFT's that suits for different OFDM systems, and realizing the processor for particular applications.

Quantum Computing and Reversible Logic:

Quantum computing holds immense potential for accelerating FFT computations. Quantumalgorithms,suchas**Shor'salgorithm**,canefficientlycomputethediscrete Fourier transform (DFT) and its inverse.

Reversiblelogicgates,whichconserveinformation,aregainingprominence.Future research could focus on designing FFT architectures using reversible gates to minimize energy dissipation and enhance performance.

Mixed-SignalandAnalog-DigitalHybrid Architectures:

Combining analog and digital components can lead to efficient FFTimplementations.Analogsignalprocessingcanhandlecontinuous-timesignals, while digital components manage discrete-time operations. Hybridarchitecturescanexploitthestrengthsofbothdomains,achievinghigh throughput and low power consumption.

Custom HardwareAccelerators:

Application-specificintegratedcircuits(ASICs)and field-programmablegatearrays

(FPGAs) can be customized for FFT computations.

Future work may involve developing specialized hardware accelerators tailored to real-valuedFFTalgorithms,optimizingresourceutilizationandreducinglatencyetc.

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