Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, April : 2024

DESIGN OF DATA FETCHER DECODER FOR SRAM USING GDI TECHNIQUE

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***Abstract*—** In this paper a new method of design of CMOS decoder circuit was proposed. To minimize power consumption and increase the performance of the design the following design solutions have been Designed the New Technique used Is Gate Diffusion Input (GDI) which need Two transistor for design of Basic gates like AND, OR gates which are used in Decoders. In this project the GDI 2-4 and 4-16 Decoder is designed and Compared with the Existing Design which is mixed-logic design method, combining transmission gate logic, dual-value logic pass-gate transistor. Three schematics are presented in the project according which 2-4 decoders were designed. In the first solution a 12-FET based circuit with GDI and 14-FET based LP Decoder and 15-FET Hp Decoders was designed which can be used to minimize the area and power consumption of digital VLSI ICs. The 12-FET based circuit was also proposed to increase the performance of digital ICs with reference to 14-FET and 15-FET based solution. Using the above-mentioned cells, the following more complex digital decoders have been designed: like 4-16 decoders. The above GDI proposed solutions have shown better performances, lower power consumptions and less required area of silicon compared to the ones currently used in digital designs. The proposed solutions have been analyzed in TANNER EDA Software.

Index Terms — CMOS, Delay, Digital, Low-power design, Performance, VLSI.

I. INTRODUCTION

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits [1]. They consist of complementary NMOS pulldown and PMOS pull up networks and present good performance as well as resistance to noise and device variation. Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

There are several types of binary decoders, but in all cases a decoder is an electronic circuit with multiple input and multiple output signals, which converts every unique combination of input states to a specific combination of output states. In addition to integer data inputs, some decoders also have one or more "enable" inputs. When the enable input is negated (disabled), all decoder outputs are forced to their inactive states.

Depending on its function, a binary decoder will convert binary information from n input signals to as many as 2^n unique output signals. Some decoders have less than 2^n output lines; in such cases, at least one output pattern may be repeated for different input values.

A binary decoder is usually implemented as either a stand-alone integrated circuit (IC) or as part of a more complex IC. In the latter case the decoder may be synthesized by means of a hardware description language such as VHDL or Verilog. Widely used decoders are often available in the form of standardized ICs.

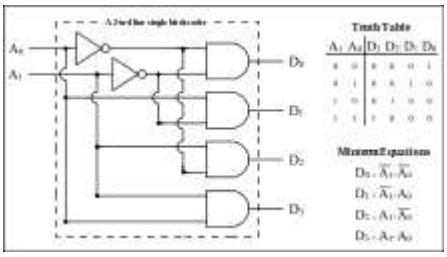

Figure - 1: A 2-to-4 line decoder

II. RELATED WORK

Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power-

efficient than complementary CMOS. However, new comparisons performed on more efficient CMOS circuit realizations and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products. An implemented 32-b adder using complementary CMOS has a power-delay product of less than half that of the CPL version. Robustness with respect to voltage scaling and transistor sizing, as well as generality and ease-of-use, are additional advantages of CMOS logic gates, especially when cell-based design and logic synthesis are targeted. This paper shows that complementary CMOS is the logic style of choice for the implementation of arbitrary combinational circuits if low voltage, low power, and small power-delay products are of concern.

A 3.8-ns, 257-mW, 16*16-b CMOS multiplier with a supply voltage of 4 V is described. A complementary pass-transistor logic (CPL) is proposed and applied to almost the entire critical path. The CPL consists of complementary inputs/outputs, an nMOS pass-transistor logic network, and CMOS output inverters. The CPL is twice as fast as conventional CMOS due to lower input capacitance and high logic functionality. Its multiplication time is the fastest ever reported, even for bipolar and GaAs ICs, and it can be enhanced further to 2.6 ns with 60 mW at 77 K.

III. OVERVIEW OF LINE DECODER CIRCUITS

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the m to 2n minterms of n input variables.

a) 2-4 Line Decoder

2-4 NAND decoder generates the 4 minterms D0-3 of 2 ascribe variables A and B. Its argumentation operation is abbreviated in Table I. Depending on the ascribe combination, one of the 4 outputs is called and set to 1 while the others are set to 0. An inverting 2-4 decoder generates the commutual minterms I0-3, appropriately the called achievement is set to 0 and the blow are set to 1, as apparent in table 2.

Table - 1: Truth Table of the 2-4 decoder

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 2: Truth table of the inverting 2-3 decoder

A	B	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

IV. METHODOLOGY

The primary issues in the design of adder cell are area, delay and power dissipation. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. This paper mainly presents the design of 5 different full adder topologies using Modified Gate Diffusion Input Technique. This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. This paper focuses two main design approaches. The former presents the implementation of modified primitive logic cells and its performance issues were compared with GDI and CMOS logic. The latter presents the implementation of 5 different modified GDI full adders and its performance issues. The simulation results reveal better delay and power performance for the proposed modified GDI full adders when compared with the existing GDI technique, CMOS and pass transistor logic at 45 nanometer CMOS technologies. Delay and power has been evaluated

by Tanner simulator using TSMC BSIM 45 nanometer technologies.

The main contribution of this proposed system presents the design of modified primitive cells and five different topologies for full adders at circuit level implemented based on the GDI technique. The modified GDI primitive cells are constructed and its significant variation between CMOS and conventional GDI are compared. Though GDI technique offers low power, less transistor count and high speed, the major challenges occurs in the fabrication process. The GDI technique requires twin-well CMOS or Silicon on Insulator (SOI) process to realize a chip which increases the complexity as well as the cost of fabrication.

a) GDI primitive cells

The basic primitive of GDI cell consists of nMOS and pMOS containing four terminals G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of MOS transistor), and D (common diffusion node of both transistors). In this work a modified primitive GDI logic gates have been implemented in 0.250μm technology and it is compared with existing GDI and CMOS logic. Figure shows the construction of modified GDI basic gates of AND, OR, NOR, NAND, XOR, XNOR and MUX. As an example the operation of AND gate is elucidated. For AND gate the drain of pMOS is -off. -off and nMOS in linear pMOS in linear and nMOS in cut-off linear and nMOS in linear thereby producing the output as 1. The logical level for different input combination will be:

For A=0 and B=0: pMOS in Linear: Vin Vtp < Vout < VDD. nMOS in Cut-off: Vin<Vtn

For A=1 and B=0: pMOS in Cut-off: Vin > VDD + Vtp. nMOS in Linear: 0 < Vout < Vin – Vtn

For A=0 and B=1: pMOS in Linear: Vin Vtp < Vout < VDD. nMOS in Cut-off: Vin<Vtn

For A=1 and B=1: pMOS in linear: Vin Vtp < Vout < VDD. nMOS in linear: 0 < Vout < Vin - Vtn

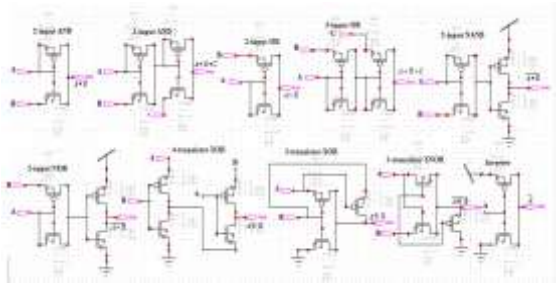

Figure - 2: GDI primitive logic gates

The performance analysis of GDI and CMOS logic is presented. The performance evaluation is made with respect to switching delay, transistor count and average power consumed by MGDI, GDI and CMOS logic. From this analysis it is observed that the modified GDI performance is better when comparing to GDI and CMOS logic.

b) Design of GDI Full adders

A full adder is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry in, C, from a previous addition produces the corresponding SUM, S, and a carry out, CARRY. The various equations for SUM and CARRY are given below

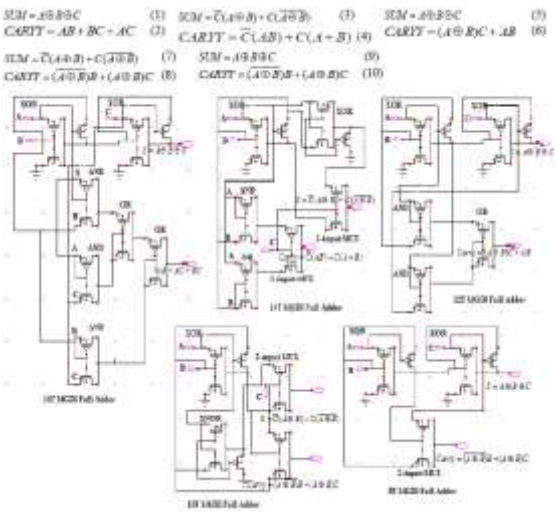

Figure - 3: GDI Full adders

Five different GDI full adders have been designed with transistor count of 16T, 14T, 12T, 10T and 8T. For 16T GDI full adder implemented from the eq 1 & 2, the sum expression is designed using 3-input XOR gate, whereas carry expression is designed using 2-input AND and 3-input OR gate.

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Similarly for 14T GDI full adder from the eq 3 & 4, the sum is implemented with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is implemented with 2-input AND and 2-input OR gate. For 12T GDI full adder from the eq 5 & 6, sum is realized using 3-input XOR gate and carry is realized using 2-input OR and 2-input AND. The 10T MGDI full adder from the eq 7 & 8, sum is designed with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is designed with 2-to-1 MUX. Finally 8T GDI full adder from the eq 9 & 10, has been realized using 3-input XOR for sum expression and for carry expression 2-to-1 MUX have been used. The proposed 5 different GDI full adders are simulated using Tanner EDA with BSIM3v3 250nm technology with supply voltage ranging from 1V to 5V in steps of 0.5V. All the full adders are simulated with multiple design corners (TT, FF, FS, and SS) to verify that operation across variations in device characteristics and environment. The design of 5 different full adders using GDI is shown in above figure.

V. RESULTS

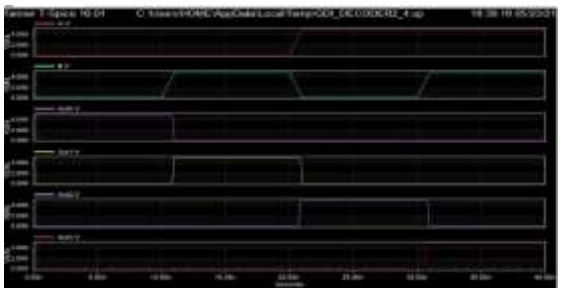

Figure – 4: 2-4 decoder Waveforms

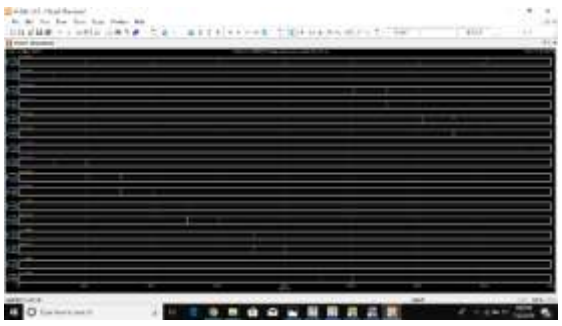

Figure – 5: 4 -16 decoder waveforms

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Power Results

VV1 from time 0 to 4e-008
Average power consumed -> 4.716174e-006 watts
Max power 2.805952e-003 at time 2.08079e-008
Min power 0.000000e+000 at time 0

VV2 from time 0 to 4e-008
Average power consumed -> 4.307109e-006 watts
Max power 2.885376e-003 at time 2.04305e-008
Min power 0.000000e+000 at time 0


Measure information will be written to file "C:\Users\HOM

Measurement result summary
   Delay            =   15.0057n
```

Figure – 6: Existing HP 2-4 decoder power Delay

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Power Results

VV1 from time 0 to 4e-008
Average power consumed -> 1.731682e-005 watts
Max power 1.311620e-003 at time 2.06787e-008
Min power 0.000000e+000 at time 0

VV2 from time 0 to 4e-008
Average power consumed -> 1.773903e-005 watts
Max power 1.109085e-003 at time 3.06631e-008
Min power 0.000000e+000 at time 0


Measure information will be written to file "C:\Users\HOM

Measurement result summary
   Delay            =   15.1661n
```

Figure – 7: GDI power Delay 2-4 decoder

Figure – 8: GDI power Delay 3-8 decoder

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Average power consumed -> 3.027209e-005 watts
Max power 5.814454e-003 at time 8.07476e-008
Min power 0.000000e+000 at time 0

VV2 from time 0 to 1.6e-007
Average power consumed -> 3.338708e-006 watts
Max power 1.624693e-003 at time 4.09657e-008
Min power 0.000000e+000 at time 0

VV3 from time 0 to 1.6e-007
Average power consumed -> 1.125754e-004 watts
Max power 5.871028e-003 at time 6.07635e-008
Min power 0.000000e+000 at time 0

VV4 from time 0 to 1.6e-007
Average power consumed -> 1.717300e-006 watts
Max power 1.592297e-003 at time 1.30958e-007
Min power 0.000000e+000 at time 0
```

Figure – 9: GDI power Delay 4-16 decoder

CONCLUSION

The proposed decoders are asymmetric and need to be properly connected to avoid hazards. For the

correct connection of the inputs, a method has been developed in TCL language, which allows to make the most of the advantages of proposed asymmetric circuits.

REFERENCES

[1] Petrosyan O.H., Avdalyan N.B., Julhakyan H.K. The new method development for construction of low power consumption decoders // Proceedings of the Tenth International Conference "SEMICONDUCTOR MICRO - AND NANOELECTRONICS", september 11-13 2015.- Yerevan, Armenia, 2015. - P. 157-163.

[2] B. Madhuri, R. Prabhakar, M.Tech. Design of Low-Power HighPerformance 2-4 and 4-16 Mixed-Logic Line Decoders. International Jurnal of Professional Enginering studies. Volume 9 /Issue 5 / Mar 2018. –p. 286-292.

[3] Dimitrios Balobas and Nikos Konofaos. Design of Low-Power HighPerformance 2–4 and 4–16 Mixed-Logic Line Decoders. IEEE Transactions on Circuits and Systems - II: Express Briefs, Vol. 64, No. 2, February 2017. – p. 176-181.

[4] Chaitanya Kommu, Dr. A. Daisy Rani. The Mixed Logic Style based Low Power Combinational circuits for ASIC designs at 32nm Technology. Compliance Engineering Journal. Volume 10, Issue 9, 2019. –p. 388-399.

[5] Bondapalli Jayanthi, B Teena Ratna Prasuna. Design of Low-Power Highperformance 2–4 and 4–16 Mixed-Logic Line Decoders. EPRA International Journal of Multidisciplinary Research (IJMR) Peer Reviewed Journal. Volume: 5 | Issue: 7 | July 2019 || SJIF Impact Factor: 5.148. –p.146-153.

[6] Ayesha, G. Aruna Kumarl. Design of Low Power, High Performance 2- 4 and 4-16 Mixed Logic Line Decoders. International Jurnal of VLSI Sistem. Design and Communication Sistems. V.05, Issue.09, September-2017. – P. 0940-0945

[7] B. Srikanth, M. Sri Hari, D. Praveen Kumar, G. Shravan Kumar. Design And Implementation of Low-Power, High-Performance 2-4- and 4-16-Line Decoders using Adiabatic Logic Circuits. International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-9 Issue-1, October 2019. –p. 2894-2901.

[8] Grande NagaJyothi, Gorantla Anusha, Kundu Debanjan. Low Power Design of 2–4 and 4–16 Line Decoders. International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-9, July 2019. P. 1220-1224.

[9] Hspice Reference Manual, Synopsys Inc.- 2017. -846p.

[10] CosmosScope User Guide Synopsys Inc.- 2011.-54p

[11] Galaxy Custom Designer Schematic Editor User Guide, Synopsys Inc.- 2014. 236p.