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LOW POWER 3-BIT ENCODER DESIGN IN DTCMOS LOGIC

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ABSTRACT:

In this paper, we are proposing one of the combinational circuit 3-bit encoder using DTMOS Structure in Memristor Logic. The configuration of DTMOS offers better results than conventional designs of encoder. A comparative analysis also has done among these configurations of design. From this analysis, weareable to choose best configuration of design that applicable for specified areas of applications.

Keywords: DTCMOS, Memristor, Pseudo NMOS logic, CMOS logic, Combinational circuits, Encoder.

INTRODUCTION:

In the era of big data protection is vita land challenging because no one can predict where and when the next down time will occur. Data backup technology is one of the best solutions in practice to minimize data loss and other negative impacts. Therefore, the efficiency in data backup and restoring will determine whether the system can maintain a continuous sand stable operation. During the backup process, data stored in the volatile memory will be transferred to the nonvolatile memory and restored after downtime ends. The latency for the data transportation mainly depends on the type of memory and the structure of the system. How to minimize such latency becomes crucial for the efficiency of data backup.

MEMRISTOR:

Memristor (abbreviation of "memory resistor") is one of such emerging memories. It waspredictedbyLeoChuain1971[1]and coinedbyHPlabin2008[2]. This passive device has been explored to have multiple advantages such as nonvolatile, high density, low power consumption, high integration, and good compatibility with CMOS devices. It has also been discovered that the use of memristors in memory components enables the volatile memory to store its intermediate states with high speed at a low cost.

Sofar,todesignelectroniccircuits,passiveelementslikeascapacitors,resistors,andinductors are used, but a fourth fundamental element also exists, which is called a "memristor". Memristance is simply charge-dependent resistance and the unit of the memristor is the ohm.

As a hypothetical non-linear passive two-terminal electrical component, the concept of memristor was first proposed based on the perspective of the circuit integrity [1]. Memristor has the

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notable nonvolatility property of having the memory of how much electric charge has flowed and in which direction through it in the recent past, which determines its present resistance. When the electric power supply is turned off, the memristor remembers its most recent resistance until the power is turned on again. This property can then be exploited to build a nonvolatile memory component. Since the first practical memristor model was built by HP Labs [2], many other models have been proposed to characterize the electrical characteristics of memristors in terms of voltage, current, and state variables in different application scenarios. A detailed description of these models can be found in an ISQED survey [8].

We adopt the voltage-controlled memristor model [9] in which the resistance of the memristor (i.e., memristance) can be switched abruptly from one value to another around the threshold voltage. The symbol of memristor is shown in Figure1.Theright terminal, denoted by the bold black bar, is called the negative terminal. The left terminal is called the positive terminal. When positive voltage is greater than the positive threshold, Vset, the resistance state of the memristor will switch to Ron, which is known as the Low Resistance State (LRS). When the negative voltage on the memristor is smaller than the negative threshold, Vreset, the resistance state of the memristor will switch to Roff, also called High Resistance State (HRS). Otherwise, the resistance of the memristor remains unchanged. The difference in the resistance values between Roff and Ron is several orders of magnitude. Such property makes it suitable to store binary values and implement nonvolatile devices.

BASIC STRUCTERE OF MEMRISTOR:

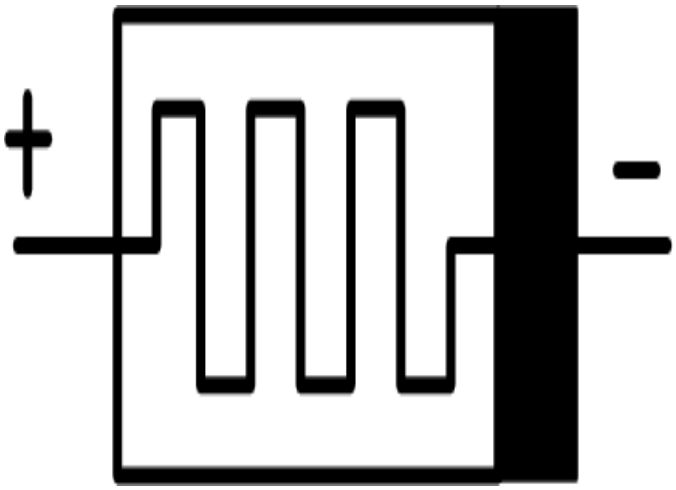

Fig1.1:The Symbol of Memristor

A memristor is an electrical component that limits or regulates the flow of electrical currentinacircuitandrememberstheamountofchargethathaspreviouslyflowedthroughit. Memristors are important because they are non-volatile, meaning that they retain memory without power.

The original concept for memristors, as conceived in 1971 by Professor Leon Chua at the University of California, Berkeley, was a nonlinear, passive two-terminal electrical component that linked electric charge and magnetic flux.

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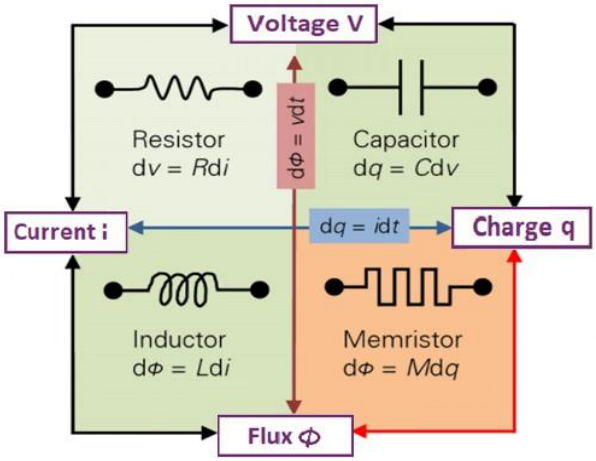

Fig1.2: Passive Two-Terminal Electrical Component

Since then, the definition of memristor has been broadened to include any form of non-volatile memory that is based on resistance switching, which increases the flow of current in one direction and decreases the flow of current in the opposite direction.

NEED OF MEMRISTOR:

A memristor is often compared to an imaginary pipe that carries water. When the water flows in one direction, the pipe's diameter expands and allows the water to flow faster -- but when the water flows in the opposite direction, the pipe's diameter contracts and slows the water's flow down. If the water is shut off, the pipe retains its diameter until the water is turned back on. To continue the analogy, when a memristors power is shut off, the memristor retains its resistance value. This would mean that if power to a computer was cut off with a hard shut down, all the applications and documents that were open before the shutdown would still be right there the screen when the computer was restarted.

Memristors, which are considered to be a sub-category of resistive RAM, are one of several storage technologies that have been predicted to replace flash memory. Scientists at HPL a is built the first working memristor in 2008 and since that time, research large IT companies have explored how memristors can be used to create smaller, faster, low- power computers that do not require data to be transferred between volatile and non-volatile memory. If the storage heirarchy could be flattened by replacing DRAM and hard drives with memristors, it would theoretically be possible to create analog computers capable of carrying out calculations on the same chips that store data.

Memristors have several attractive features that make them compelling for computer scientists: They require less energy to operate and are faster than present solid-state storage technologies and they can store at least twice as much data in the same area. Memristors are virtually immune from radiation, which can disrupt transistor-based technologies. Also, memristors can enable computers that turn on and off like a light switch.

Different from an electrical resistor that has a fixed resistance, a memristor possesses a voltage-dependent resistance, which means that a material's electric properties are key. A memristor material must have a resistance that can reversibly change with voltage. Memristors have a very simple structure – often just a thin film made of titanium dioxide between two metal electrodes.

Industrial Engineering Journal
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ENCODER:

An Encoder is a combinational circuit that performs the reverse operation of Decoder. Maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

PSEUDO NMOS:

Pseudo-NMOS logic uses only one PMOS device as a pull-up device for a multi- transistor N-Logic block. Therefore, the required number of transistors for a N input gate is an N+1 transistor. The used PMOS device has its gate connected to ground and
is therefore always "ON". When the N-Logic block is "OFF", the output is charged to Vdd. When the N-block is "ON", a large current can pass from Vdd to ground, causing large power consumption. Device dimensions, for Pseudo-NMOS, must be carefully chosen to allow the output to be discharged to ground. The PMOS device must be chosen wide enough to conduct a multiple of the N-block's leakage current when the output is "high", and narrow enough so that the N-block can still pull down the output safely. Therefore, Pseudo-NMOS logic is a ratioed logic.

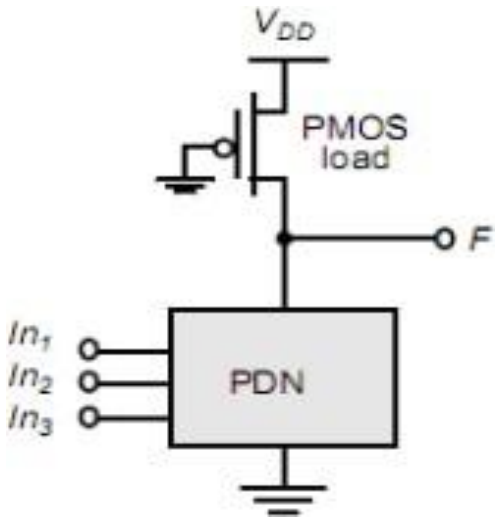

Fig1.3: Block Diagram of Pseudo-NMOS Logic

Pseudo-NMOS logic has the advantage of higher speed than static CMOS logic; especially in large fan-in NOR gates. This is due to the fact that there is only one PMOS transistor contributing for the output rise time. The overall speed improvement is substantial, at the cost of a slight increase in power consumption.

EXISTING METHODOLOGY:

Information in digital logic circuits with specific meaning is encoded in to corresponding binary bits. Encoder is a circuit which does this encoding function. The encoder's function is to encode when one of the input bits is of effective level, and the encoder's output changes in accordance with its input bits. The circuit has 'N' outputs and 'M' inputs and they are related by M = 2N.

Industrial Engineering Journal
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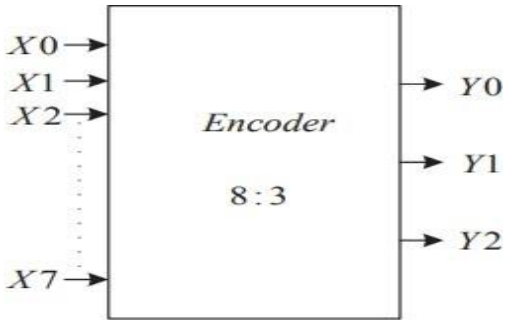

Fig3.1: BlockDiagramOf3-bit Encoder

X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Table3.1: Truth Table of Encoder

From the Encoder truth table, the outputs and inputs are related by

Y0=X1+X3+X5+X7

Y1=X2+X3+X6+X7

Y2 =X4 +X5+X6+X7

From these relations, logic circuit can be implemented using CMOS, Pseudo NMOS and MRL. In the Encoder circuits, X1-X7 are input bits and Y2, Y1, Y0 are output bits. In Encoder circuit by using MRL, M1, M2, M3, M4 act as pull-down network and a Memristor acts as pull-up network. M1, M2, M3, M4 and Memristor constitute a 4-input NOR gate. X1, X3, X5, X7 are the input signals that pass through the NOR gate and the signal at the drain of M1 is inverted signal of (X1 + X3 + X5 + X7). M13 and Memristor constitute an inverter. The output of 4- input NOR gate is given as the input of inverter. The signal at the drain of M13 is Y0 = X1 + X3 + X5 + X7.

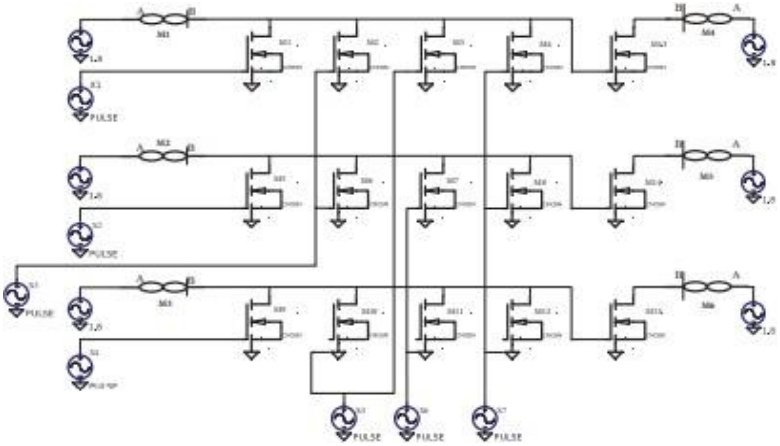

Fig3.3: Schematic of Encoder Using CMOS Logic

Industrial Engineering Journal
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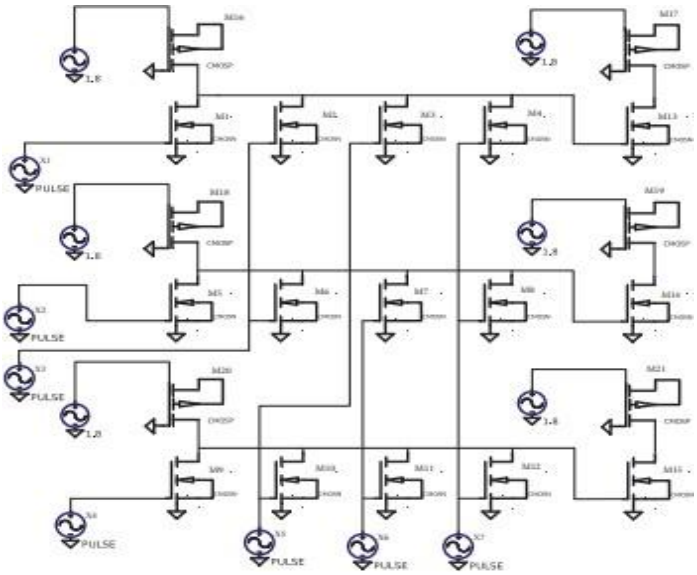

Fig3.4: Schematic of Encoder Using CMOS Logic

s, it is known that the area occupied by a Memristor based design is lesser than CMOS [11], [14], [15], it can be depicted that this design is efficient with respect to the area consumed. The number of transistors that are required for this design is the least when compared to the conventional CMOS and Pseudo NMOS logic. By using CMOS technology, the encoder circuit has 30 transistors, of which 15 PMOS and 15 NMOS. By using Pseudo NMOS technology, the encoder circuit has 21 transistors, of which 5 PMOS and 15 NMOS. By using MRL technology, the encoder has 21 transistors, of which 6 Memristors and 15 NMOS.

PROPOSED METHOD:

In this chapter, the structure of DTCMOS is discussed in detail. Here, the modifications are made in the design of encoder using Memristor. The transistor configurations in the modified code is done by using DTCMOS structure. The main advantage of this DTCMOS configuration is it offers fast performance than the conventional designs of encoder.

DTCMOS:

The DTCMOS technique is mostly used in digital applications in which the gate and body of the MOSFET are tied together. This is to reduce the leakage current during off state and reducing the threshold voltage during on state to increase the overdrive voltage. It is also possible to use the DTCMOS technique in bulk CMOS technology for analog circuit applications. However, in analog applications the body terminal of the MOSFET transistor is normally used as a fourth terminal.

In the standard bulk CMOS technology, it is possible to use the body of PMOS transistors as a fourth terminal to the MOSFET. By changing the absolute value of V_{bs} from 0 to 0.5 V, the threshold voltage reduces by more than 25%. Increasing V_{bs} also causes drain current to increase. However, note that as the body-source junction becomes more forward biased, more current goes into the body terminal of the MOSFET [Fig. 1(c)], which is not desirable. A forward bias of up to about 0.4 V is acceptable. Even for a forward bias of 0.5 V, the body current is still much smaller than the drain current and can be ignored in many applications.

Several issues should be considered while using the bulk as the fourth terminal of the transistor.

Industrial Engineering Journal
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First, the bulk terminal has a lower trans-conductance gmbcompared to gate trans-conductance. Second, the parasitic capacitance of the bulk terminal can be larger than that of the gate. This is due to the relatively large area of then-well in which the PMOS transistor is formed. Therefore, body terminal should not be part of a high frequency path. Finally, the forward bias voltage of the body terminal should not exceed a fraction of a volt.

The DTCMOS technique can have several advantages in low-voltage analog circuits. First, in low-voltage applications there is not much voltage headroom for signal swing and reducing the threshold voltage can be helpful. Second, having a fourth terminal can be advantageous since it can result in a simpler circuit with a fewer number of transistors. Third, the voltage range at the body terminal of a PMOS transistor normally covers the range of voltages which is not covered by the gate of the transistor. Therefore, using the bulk terminal makes it possible to extend the input voltage range of a circuit.

PROPOSEDDESIGN:

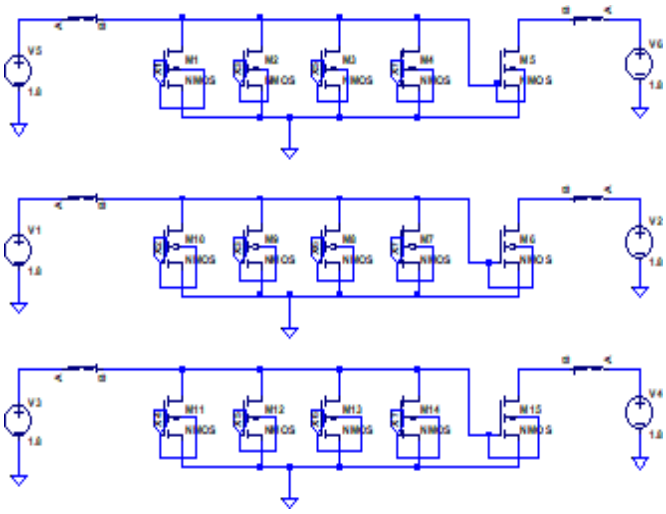
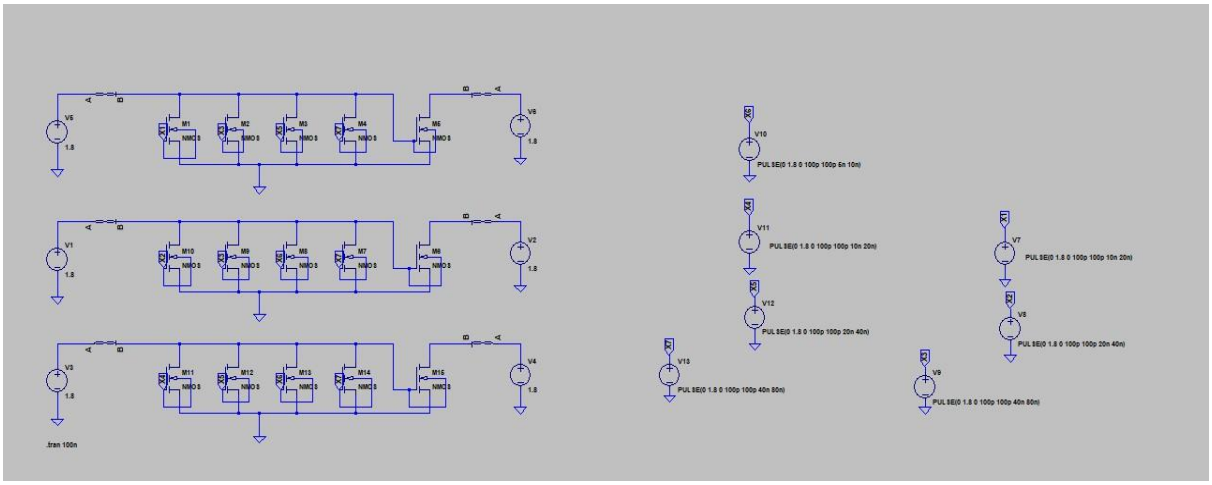


Fig5.1: Schematic of Encoder Using DTCMOS Logic

RESULTS:



Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, No. 3, April : 2024

Fig8.1: Schematic of Encoder Using DTCMOS Logic

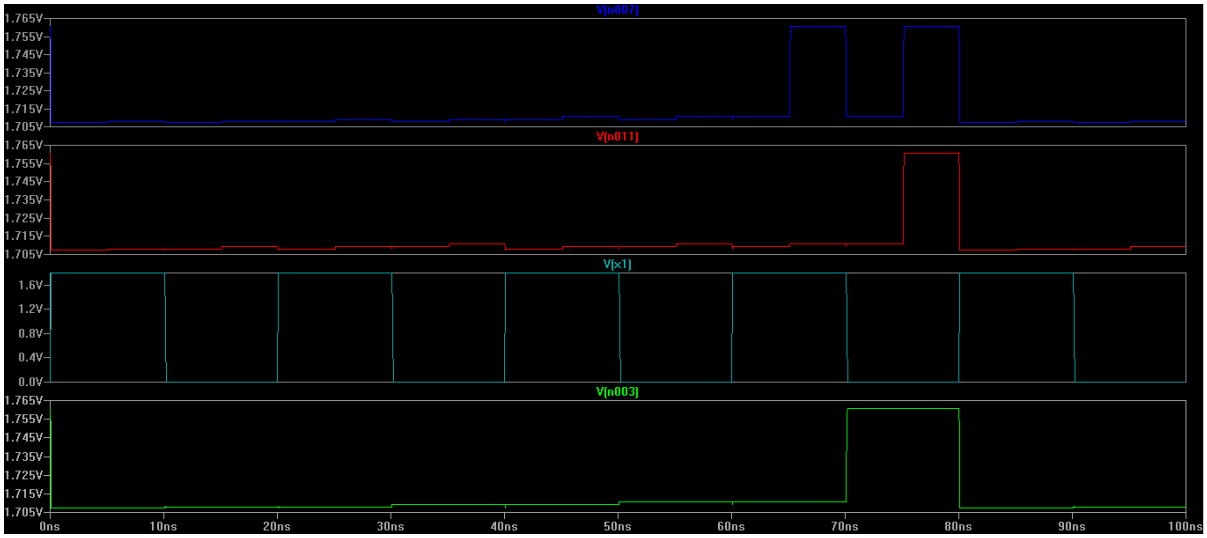


Fig8.2: Output Waveforms of Proposed Design

Comparison of performance parameters among CMOS, Pseudo NMOS and MRL based encoders.

Types Of Encoder	**Avarage Power**	**Delay**
CMOS based encoder	12.94µW	154.083ps
Pseudo NMOS encoder	149.93µW	77.5194ps
MRL based encoder	563µW2	77.0416ps
MRL based encoder using DTCMOS	695.07nW	77.5194ps

Table8.1: Comparison of Performance

CONCLUSION:

Design of encoder with Memristor and DTMOS based logic design is much efficient in the aspects of power and area when compared with conventional CMOS logic and Pseudo NMOS logic. The trade-off between the power, area and speed of a circuit is persistent. It can be concluded that this design technique gives lesser number of transistor count required and makes it more efficient way of designing a digital circuit.

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