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MULTI-CHANNEL UART USING FPGAIMPLEMENTATION

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***Abstract*—** In this paper a universal asynchronous receiver and transmitter (UART) are described, which is basically a serial data transmission protocol used in digital circuit applications. The architecture of the UART transmitter has a baud rate generator, parity generator, transmitter finite state machine (FSM) and parallel in serial out register (PISO). UART receiver has a baud rate generator, negative edge detector, parity checker, receiver finite state machine (FSM) and serial in parallel out (SIPO) register. The baud rate generator of both transmitter and receiver is the same, so the baud rate of transmitter/receiver is the same. Baud rate generator is the same as the frequency divider circuit. The data frame of the UART transmitter is 1 start bit, 8 transmits data bits, 1 parity bit and 1 stop bit. The baud rate of the transmitter and receiver is 4 Mbps using the system clock of 64 MHz's.

Keywords: UART, Baud Rate Generator, Asynchronous FIFO, Simulation

I. INTRODUCTION

UART is a popular methodology of serial asynchronous communication. The UART data frame is composed of a start bit of one bit-length logic 0, 5 to 8 bit-length data bits and a stop bit of one, one and a half or two bit-length.There may be one bit-length checkout bit after the data bits if it is necessary[8]. Communication is a very effective process that affects the system's performance. UART is the one of the module used for communication between two sub equipment and it is a more commonly used serial communication protocol than SPI and I2c protocols[3].

A UART is an integrated circuit that handles the conversion between serial and parallel data and is suitable for long-distance communication, because it needs only a few transmission lines. Serial communication diminishes the distortion of a signal so making data transfer between two systems parted over a long distance.Parallel communication requires a lot of multi-bit address buses and data buses and uses more transmission lines compared to serial communication and it is only suitable for short-distance datatransmission only[2].

But, using a single UART does not satisfy and support complex communication with different Baud rates because a single UART operates with a specific Baud rate, and while in communication process data loss may occur due to different baud rates and differences in transmission speed which causes bit error. To communicate with different baud rates of systems, A multi-channel UART controller is designed and implemented using FPGA in this paper. This, Multichannel UART involves Four UART channels each one is operated at a different Baud rate[7]. Depending on the requirement user can select any one of the UART from these 4 UART Channels. The multi- channel UART is designed by using Asynchronous FIFO which reduces the delay. The most important advantage included in this multi-channel UART controller [5,6]can operate in parallel i.e., more devices can be able to communicate with the systems.

II. DESIGN OF MULTI-CHANNEL UART

The architecture of the uart transmitter is described. Figure describe the architecture of the uart transmitter. Uart transmitter architecture is the integration of the following modules.

The Multi-channel UART has four individual UARTs each UART have two pins XOUT and XIN and each UART is connected to the controller shown in figure1. At the transmitter end and receiver end of the controller FIFO is connected to overcome the data loss and the transmission between the controller and FIFO is a full-duplex

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transmission [4,8]. Here, the Baud rate generator is also included in this controller which is used to measure the Baud rate of a UART. Depending on the user application or requirement user can select any one of UART.

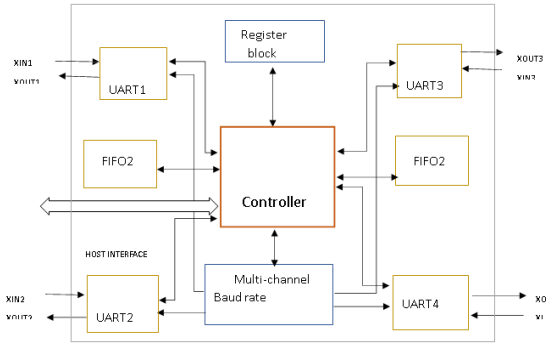

Figure - 1: Multi-channel UART

III.BAUD RATE GENERATOR

A Baud rate generator is a clock generator and is used to measure the data rate at which the data transmitted by a UART is possible. In serial communication at the transmitter side and receiver side, the duration of a bit is synchronized by this Baud rate generator hence, it is also known as a programmable bit timing device. By generating a pulse this baud rate generator calculates the baud rate of each UART. The formula for the Baud rate can be obtained as follows.

Baud rate = Bit rate/Number of bits

To receive the data width of 16 times the receiver clock cycle, This Baud rate generator is designed generate the frequency of the receiver clock to 16 times the baud rate.

IV.ASYNCHRONOUS FIFO

It is defined as the clock domains in the FIFO which are asynchronous to each other meaning that the read and write clocks of FIFO are not Synchronized to each other. In this, reading the data from the FIFO and writing the data to the FIFO are having different rates. Since the read and write clocks of the data bus and UART's clock are not the same this causes data loss and also there may be a chance of getting probability of bit error. The main purpose of FIFO is to send and receive data from one clock domain to another. The clock domain and reduces the interaction time between the serial port and the CPU which improves the transmission efficiency and synchronizes the data flow between the sub-equipment[9].

This asynchronous FIFO contains the read pointer, write pointer, empty flag, and full flag. The FIFO sends a FULL signal or an EMPTY signal to indicate whether the FIFO is full to write data or empty to read data. The clear signal is used to erase the data from the asynchronous FIFO.

V. BIST TECHNOLOGY

Built-In-Self-Test(BIST) which allow IC to perform self-testing, this technology helps to design hardware and software features into the IC. It reduces the usage of external systems [5-6] by testing itself using its circuits itself. It is also called as Design- For- Testability (DFT) technique. BIST circuits contain memory and logic BIST for memory and logic circuit testing. BIST solution consists of a Test Pattern Generator (TPG), a circuit to be tested, a way to analyze the results, and a way to compress those results for simplicity and handling.

In this, it provides easy, faster, and efficient electrical testing of a chip with less cost.

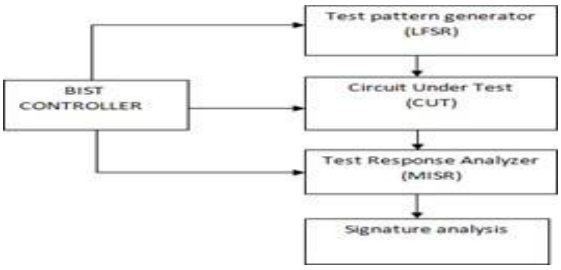

Figure - 2: UART with BIST

VI. VERIFICATION OF RESULT

UART Transmitters Simulation:

The UART transmitter consists of Buffer Register & Shift Register. The Shift Register consists of a start bit, stop bit, parity bit, and 8 bits of data. The shift register bits are shifted to the receiver's shift register bit by bit. The figure3 shows the output

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waveforms of the UART transmitter.

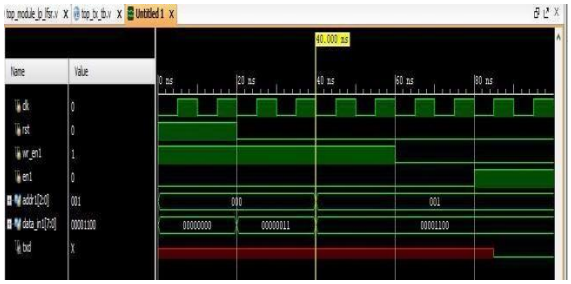

Figure - 3: UART Transmitter

Receivers Simulation Results:

During the receiver's simulation process, the system clock frequency is set to 32MHz, and the baud rate of UARTs maintained at 9600bps, 19200bps, 38400bps, and 4800bps respectively. Fig 6 shows the simulation results of multiple receivers with different baud rates.

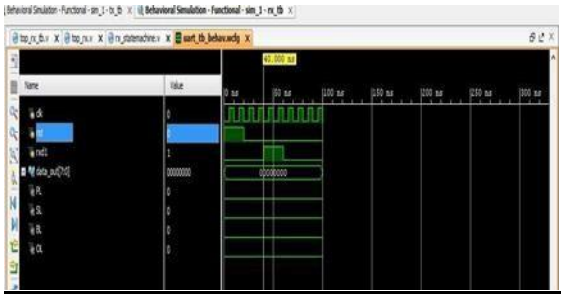

Figure - 4: UART receiver

Simulation Results of FIFO at Transmitters and Receivers:

The simulation results of FIFOs are obtained by using the model Sim software. Fig 7 shows the simulation result of FIFOs which are placed at the receiving and transmitting ends.

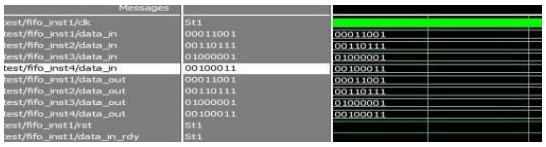

Figure - 5: Simulation results of FIFO

Simulation result of UART:

The verification of multi-channel UART is verified using the simulation waveform of the UART transmitter and receiver and the synthesis result is verified in the 14.7 version of Xilinx Software.

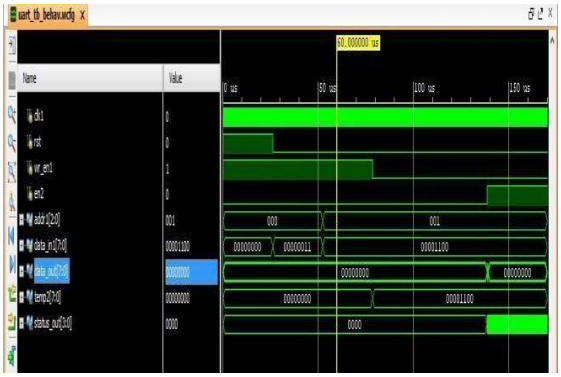

Figure - 6: UART Output Waveform 1

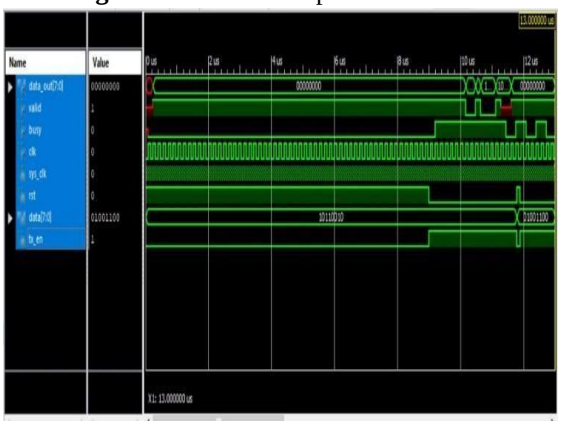

Figure - 7: UART Output waveform 2

CONCLUSION

The conclusion of this project is to Design, Simulation, Synthesis, and Implementation of a Multi-channel Universal Asynchronous Receiver and Transmitter (UART) is successfully verified using Very High-Speed Integrated Circuit Hardware Descriptive Language (VHSIC-HDL). The multi-channel UART controller meets the communication needs of a multi-part control system. The design has great flexibility, high integration, and high reliability. Because of using Asynchronous FIFO data loss will be reduced. In this project, BIST technology is proposed to avoid errors. This multi-channel UART also reduced the time delay between master and slave equipment of a multi-part control system by changing the different FPGA families and it improves the synchronization of each piece of equipment. The verification of multi-channel UART is verified using the simulation waveform of the UART

transmitter and receiver and the synthesis result is verified in the 14.7 version of Xilinx Software. The results are stable and reliable which shows the correct functionality.

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