Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, April : 2024

A POWER EFFICIENT AND DELAY OF CMOS PHASE FREQUENCY DETECTOR USING NANO DIMENSION

[1]Galipalli Dharanija,[2] Mr. G. Lakshmi Bharath, [3]R.L.B.R Prasad Reddy
[1]PG Student, Dept. of ECE, SITS, Kadapa, AP, India.
[2]Assistant Professor, Dept. of ECE, SITS, Kadapa, AP, India.
[3]Associate Professor, Dept. of ECE, SITS, Kadapa, AP, India.
[1]g.dharanija@gmail.com, [2]Lakshmibharath.414@gmail.com, [3]rajendra.409@gmail.com

Abstract — In this Project the design of phase detector circuit using nano dimensional transistor has been presented. which are mainly used in phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high- performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. The power dissipation, transistor delay, product of power and delay of the phase detector circuit has been estimated. Power and speed performance analysis is carried out varying the value of VDD in the range 1.2 V - 5V and aspect ratio of PMOS to NMOS from 1 to 5. Moreover, the power, gate delay and PDP of the phase-frequency detector has been designed. The results are pleasing context to the design of Very Large Scale Integrated (VLSI) circuit having high speed and low power dissipation.

Key Words: Phase Locked Loops (PLL), PMOS, NMOS, VLSI, Delay, CMOS logic, rise time, fall time, frequency.

I. INTRODUCTION

CMOS technology is the semiconductor technology used in the transistors that are manufactured these days. Now-a-days it is mark able invention for the electronic designers to integrate all the components in a single chip in a system. The new invention towards the technology implementation is speed of the memory increases, cost decreases and reduction of size devices. The transistor occupiers less space. The integration of MOS transistor in large multiprocessors, the sum of leakage current in bipolar transistors becoming a severe problem. The variations of leakage current increases power consumption in MOS transistors. The MOS devices work with only switching voltages in terms of power consumption. The significance of analog signals represents different conversion parameters takes place in different devices in CMOS technology.

Frequency modulation is one of the applications of the PLL, used in many devices. The feedback control circuit changes the output according to the desired application by locking the phase of the input signal. For instances, the analog signal is implemented by a digital signal with different types of devices i.e. analog to digital coverts in the design of PFD. Example comparator takes the analog input signal and it will be changing as digital signal by flip-flop and counters. The analog signals used in many different practical applications needs conversion of discrete digital signal in advance such as charge pump. In the design of PFD both analog and digital signal are used different logics are applied in the design PFD.

II. PHASE LOCKED LOOP

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CK_{ref} to produce a high-frequency clock CK_{out} this is known as clock synthesis.

A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate

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a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

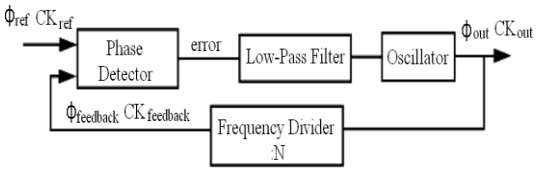

Figure - 1: Basic block diagram of a PLL

The "Phase frequency Detector" (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". The "Charge Pump" (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a "Low Pass Filter" (LPF) to generate a DC control voltage. The phase and frequency of the "Voltage Controlled Oscillator" (VCO) output depends on the generated DC control voltage. If the PFD generates an "UP" signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the contrary, if a "DOWN" signal is generated, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system.

III. PHASE FREQUENCY DETECTOR

The "Phase frequency Detector" (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". Figure shows a traditional PFD circuit.

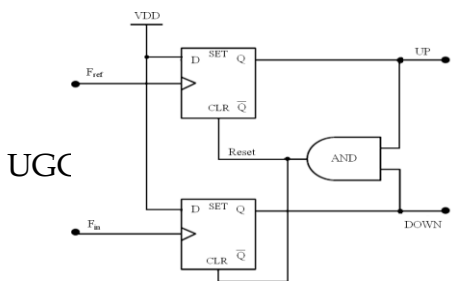

Figure – 2: Block diagram of a traditional PFD circuit

If there is a phase difference between the two signals, it will generate "UP" or "DOWN" synchronized signals. When the reference clock rising edge leads the feedback input clock rising edge "UP" signal goes high while keeping "DOWN" signal low. On the other hand, if the feedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition PFDs [6-7] are generally preferred over traditional PFD.

IV. CONVEX OPTIMIZATION OF VCO IN PLL

Geometric programming methods are special optimization problems in which the objective and constraint functions are all convex [22-24]. Convex optimization technique can solve the problems having a large number of variables and constraints very efficiently [22]. The main advantage of this method for which people generally adopt is that the method gives the global solution. Infeasibility is unambiguously detected. Since a lower bound on the achievable performance is given, so the method uses a completely non- heuristic stopping criterion.

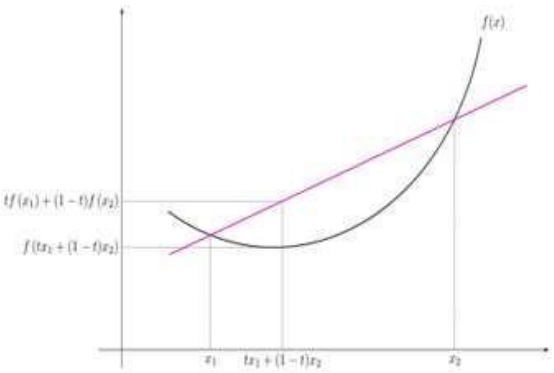

Figure - 3: Convex functions on an interval

Geometric programming is a special type of optimization technique in which all the objective must be convex. Before applying this technique it has to confirm that whether the given problem is convex optimization problem or not. Convex optimization problem means the problem of

Industrial Engineering Journal
ISSN: 0970-2555
Volume : 53, Issue 4, April : 2024

minimizing a convex function subject to convex inequality constraints and linear equality constraints. In IC integration convex optimization and geometric programming has become a more efficient computational tool for optimization purpose. This method has an ability to handle thousands of variables and constraints and solve efficiently. The main advantage of convex optimization technique is that it gives the global optimized value and the robust design. The fact that geometric programs can be solved very efficiently has a number of practical consequences. For example, the method can be used to simultaneously optimize the design of a large number of circuits in a single large mixed-mode integrated circuit.

V. DESIGN AND SYNTHESIS OF PLL

The value of the charge pump current and the component parameters of the loop filter play a major role in the design of the phase locked loop circuit. The value of the lock time mainly depends upon these parameters. So, while designing the circuit proper care should be taken in calculating these parameters. For the given values of reference (F_{ref}) and output frequency (F_{out}) as well as the lock in range, the following steps to be carried out in designing the filter circuit.

The current starved VCO design specifications are mentioned in the following table.

Table – 1: VCO design specifications

Parameter	Value
Center frequency	1GHz
No. of inverter stage	5
Inverter delay	100ps
Load capacitance	65fF
Supply voltage	1.8V

The whole PLL system design specifications and parameters are shown in the Table 2.

Table – 2: PLL design specifications and parameters

Parameter	Value
Reference frequency(F_{ref})	500 MHz
output frequency(F_{out})	1 GHz
Lock in range	100 MHz
Supply voltage	1.8 V
Divider circuit	By 2
Charge pump current (I_{puNp})	600 µA
Capacitor (C_1)	15 pF
Capacitor (C_2)	1.5 pF
Resistor (R)	1.384 K?

Table – 3: List of design parameters of the CSVCO circuit

Parameter	Value
Width of Current starved PMOS(W_{PCS})	2.33µ m
Width of Current Starved NMOS(W_{nCS})	140nm
Width of PMOS in Inverter(W_P)	2.44µ m
Width of NMOS in Inverter (W_n)	150nm
$L_{PCS} = L_{nCS} = L_P = L_n = L$	100nm

VI. SIMULATION RESULTS AND DISCUSSION

The Pass Transistor DFF PFD circuit is shown in Figure-4. The PFD is same as to a dynamic two-phase master-slave pass-transistor flip-flop. The clock skew is minimized by using single edge clocks. In this design synchronous reset is used for master while asynchronous reset is used for slave. i.e., the reset is allowed only when the slave latch is transparent.

The operating range of the design is increased with the help of synchronous resetting and also the power consumption is reduced compared to the traditional PFD. If the master latch is reset while it is transparent, then there will be significant short-circuit current will produce, resulting in more power. The output of the PFD when F_{ref} signal rising edge leads F_{in} signal rising edge and vice versa is shown in the Figure-5 and Figure-6 respectively.

Industrial Engineering Journal
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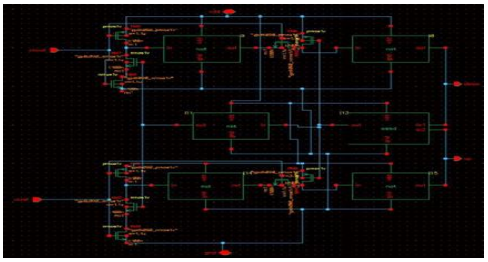


Figure - 4: Circuit diagram of a pass transistor based DFF PFD

Figure - 5: Simulation result of PFD when F_{in} rising edge leads F_{ref} rising edge

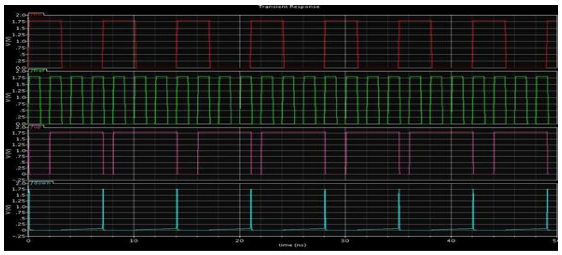


Figure - 6: Simulation result of PFD when F_{ref} rising edge leads F_{in} rising edge

a) Charge Pump and Loop Filter

When the reference signal clock edge leads the feedback clock edge, the UP signal of the PFD goes high. So, to make both the clock have rising edge at the same time the VCO output signal frequency has to be increased. For this purpose, an increase in control voltage is needed from the output of charge pump and loop filter circuit. The simulation result which is shown in the Figure-7 below gives an increase in the control voltage at the output of the loop filter circuit.

From the Figure - 8 it's clear that the control voltage increases for a period during which the UP signal of the PFD remains high. In the other case a decrease in the control voltage is produced at the output of the filter circuit which is shown in the Figure 7.5. When the rising of feedback signal leads the reference signal rising edge the control voltage decreases for the period during which the DOWN signal of the PFD remains high.

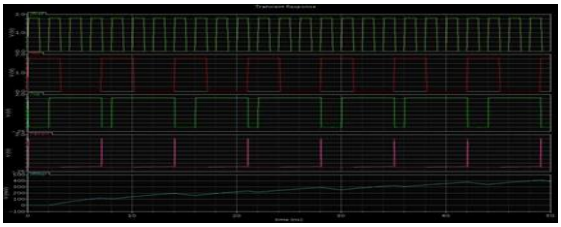


Figure - 7: Simulation result for loop filter with PFD when F_{ref} clock edge leads F_{in} clock edge

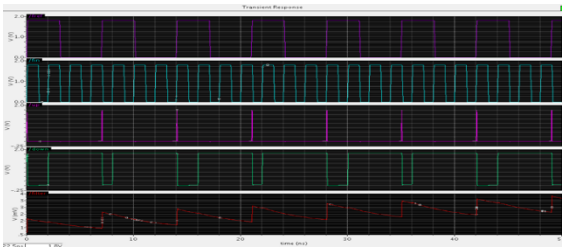
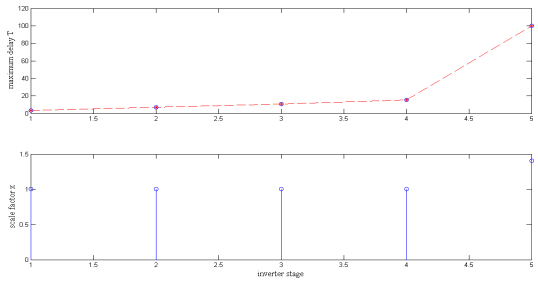


Figure - 8: Simulation result for loop filter with PFD when F_{in} clock edge leads F_{ref} clock edge

b) Result using convex optimization method

Using convex optimization method, the scaling ratio is found out to satisfy the center frequency of oscillation (i.e. delay of the circuit). The scaling ratio for different stages of the inverter in the VCO



is 1,1,1,1 and 1.4058. The scaling ratio result is shown in the Figure 9.

Figure - 9: Simulation results of scaling ratio and corresponding delay

c) Frequency Divider

The circuit diagram of a pass transistor based DFF frequency divider circuit is shown in the Figure-10. The circuit divides the frequency by a factor of 2. The simulation result of the divide by 2 circuits is shown in the Figure-11.

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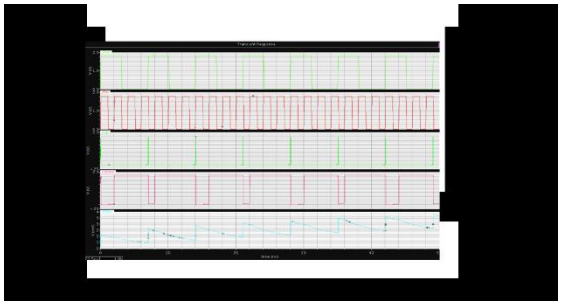

Figure - 10: Circuit diagram of a pass transistor based DFF frequency divider circuit

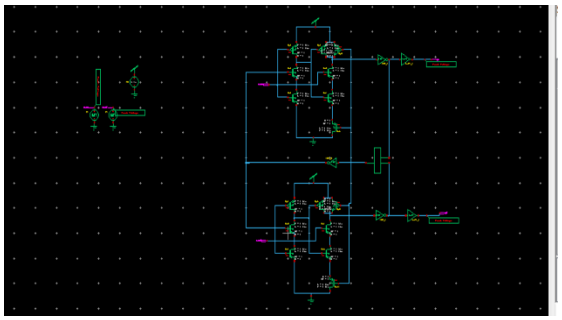

Figure - 11: Proposed Schematic New phase frequency detector

Table – 4: Performance comparison Existing and Proposed Systems

	Existing Systems	**Proposed Systems**
No. of MOSFETs	86 No's	34 No's
Power	16.44 uw	2.0 uw
Delay	497 ps	95.3159ps

CONCLUSION

In this work a PLL with a better lock time is presented. The lock time of the PLL is found to be 280.6 ns. The PLL circuit consumes a power of 11.9 mW from a 1.8 V D.C. supply the lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved. The center frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes. By applying the convex optimization technique with frequency of oscillation as the main objective function, the deviation of oscillation delay is minimized to 95.3159ps from 497 ps. Here the convex technique is used to find out the transistor sizing to meet only the desired frequency specification. The other constraints like area, power and phase noise can also be applied.

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