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LOW POWER 7T SRAM CELL DESIGN

M. Damodhar Rao, Assistante Professor,
V.V.K.D.V. Prasad, Professor,
[3]M. Sudheer Kumar Reddy, [4]N. Yogitha, [5]N. Venkata Durga Karthik and [6]P. Dhanunjay
UG Student,
Department of Electronics & Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Seshadri Rao Knowledge Village, Gudlavalleru, India
[1]damu406@gmail.com, [2]varaprasadvvkd@gmail.com, [3]sudheerkumarreddy226@gmail.com, [4]yogithanadella2002@gmail.com, [5]nvdkarthik562@gmail.com, [6]pydi.dhanunjay@gmail.com

Abstract
Static Random Access Memory (SRAM) is a vital component of modern digital systems. However, scaling down the SRAM cell size to achieve higher integration densities has led to several challenges, including reduced stability margins, increased power consumption, and susceptibility to process variations. In this study, we present a novel 7T SRAM cell architecture that addresses these issues by improving the stability margins, reducing power consumption, and enhancing the tolerance to process variations. 7T SRAM cell utilizes a combination of NMOS and PMOS transistors, and a feedback loop to maintain the cell's stability during read and write operations. The cell has been simulated using 45nm CMOS technology, and the results show a significant enhancement in stability margins and compared to a standard 6T SRAM cell, this cell consumes less power. Furthermore, the 7T SRAM cell demonstrates better performance in the presence of process variations, making it a promising candidate for future high-density memory applications.

Keywords – SRAM cell, SNM, Power dissipation, Cadence Virtuoso

I. INTRODUCTION

In recent days, semiconductor memories are the inbuilt of the device and it is an integral part of VLSI. It is making the insufficient area in the evice by occupying more area for memory. The need for smaller sizes of transistors is important for decreasing the area density of the device. This makes Improving the Technology area decreased from one level to another, which makes the device more sufficient by adding additional features, with the demand for low-power, high-speed, and highly stable memory [1]. The demand for low-power devices is more in the present day. However, scaling down the SRAM cell size has led to several challenges, such as reduced stability margins, increased power consumption, and susceptibility to procedure variations. Calculating the SNM helps the reliability of the SRAM cell.

. In this study, we present a novel 7T SRAM cell architecture that offers significant improvements in stability margins, power consumption, and tolerance to process variations in comparison to the normal 6T SRAM cell [2]. The 7T SRAM cell utilizes a combination of transistors (NMOS and PMOS) and a feedback loop to maintain stability during read and write operations [3]. By adding an additional transistor and feedback loop, the 7T SRAM cell provides better stability margins, higher read and write margins, and improved write ability comparison to the normal 6T SRAM cell [17].

The suggested 7T SRAM cell has been simulated using 45nm CMOS technology, and the results demonstrate a significant enhancement in stability margins and power consumption comparison to the

standard 6T SRAM cell [12]. Additionally, the 7T SRAM cell demonstrates better performance in the presence of process variations, making it a promising candidate for future high-density memory applications [4].

In the following sections, we will discuss the background and related work on SRAM cell design, the 7T SRAM cell architecture, the simulation results, and the conclusions of this study.

II. 6T SRAM CELL

Conventional 6T SRAM is the standard one that helps to build other topologies. A typical SRAM cell consists of six MOSFETs and operates in three modes: read, write, and hold [4]. Two cross-coupled inverters made of four transistors each hold one bit in an SRAM, while two additional access transistors allow read/write operations to be performed on a storage cell [1][13]. The data is written to Bit Line BLB and its counterpart, Bit Line BL. Q and Q' represent two nodes for storage. M5 and M6 are the two access transistors [5]. NMOS transistors M1 and M2 are pulled down while PMOS transistors M3 and M4 are pulled up. As seen in Fig 1, M1, M3, and M2, M3 are two inverters with cross-coupling pairs [15]. WL is a word line. is in charge of maintaining the cell in an active or standby mode? Its value controls whether or not access transistors are switched ON or OFF. The data is read from two complimentary Bit lines during the reading procedure. In the hold state, the word line is deactivated and the cell doesn't do anything [2].

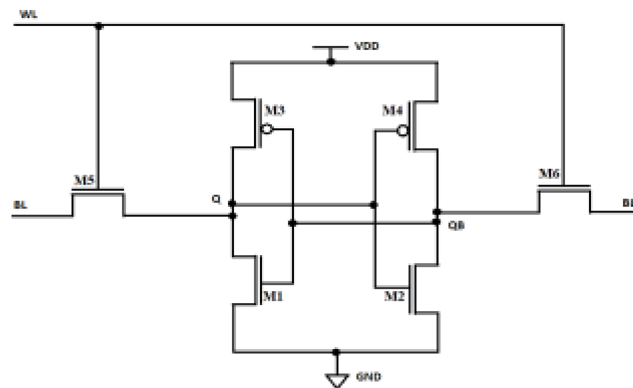

Fig 1: 6T SRAM CELL

Bit lines are pushed to complimentary voltage levels during the write operation, and then the word line is increased [3]. The data that will be entered into the cell is pushed onto the bit lines, and one of the storage nodes is ejected after passing past the access transistor [5]. The inverters that are cross-coupled increase the voltage on the opposite storage node and latch the cell. As a result, the new data overwhelms the cross-coupled inverters. The main difficulties of SRAM design are shrinking its size, as well as guaranteeing that the circuitry maintaining the state is insufficient to be overwhelmed during write cycle yet not so powerful as to be disrupted during a read cycle (read stability) [8].

Read operation can be performed by activating the word line, switches of access transistors are both closed [6]. When the cell enters state 1, the signal flows in large amounts on the bit-line and in little amounts on the complement bit-line. When a cell enters state 0, the inverse is true [7]. Finally, for both the bit line and bit line bar receive compliments. Sense/write, which is connected on the back side of two-bit lines, monitors their states and then converts them to output.

Both access transistors must be turned off for Hold Operation. SRAM maintains its state due to the existence of a latching element. The major purpose of using static RAM is to generate Cache Memory [8]. The cost of static RAM is higher. Because it has a more sophisticated structure, and its complexity is likewise limited in terms of storing a significant amount of data on a single chip [14].

A. Power dissipation

The total power lost by an SRAM cell when it is in active mode across all dynamic and static components. The standby leakage current consumes electricity when in standby mode. Dynamic power dissipation is divided into two components [9]. One source of switching power is the charging and draining of load capacitance. The other source of power is short circuit power, which is caused by the nonzero peak and fall durations of the input waveforms. The leakage current via each transistor determines a CMOS circuit's static power [15].
Static and dynamic power dissipation expressions are shown

$$P_{dy} = C \times V^2 \times f \times \alpha \text{ - - - - - - - - (1)}$$

$$P_{st} = I_{leak} \times V \text{ - - - - - - - - - - - - - - (2)}$$

Where α is the switching activity; f is the operating frequency; C is the load capacitance.

B. Static Noise Margin

SNM is a measure of an SRAM cell's capacity to keep its data stable in the face of noise [8]. SRAM is also described as the amount of noise voltage present on SRAM storage nodes that is required to flip a cell's state. SNM is determined using a graphical approach that involves sketching and reflection the inverter features and then computing the biggest square as possible between them [6].

III. NOVEL 7T SRAM CELL

In SRAM cell, the concentration of cell substrate doping needs to increased to lower the depletion width correspondingly [10]. In addition to junction scaling and gate oxide thickness, strategy for improving the engineering of short-channel characteristics is excellent, which involves scaling the same factor will affect both the device voltages and the device dimensions [4]. The potential contours and electric field distribution can be modified by modifying the doping profile in the channel area. The objective is to optimize the channel description so that leaking in the off-state is minimized while linear and saturation driving currents are maximized [5]. These are the ways to reduce leakage at the process level.

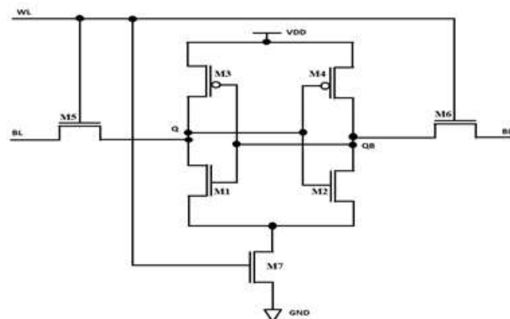

Fig 2: 7T SRAM CELL

At the circuit level, there are different approaches to minimize the leakage power by using various approaches like self-reverse biasing, multiple Vth design, multiple channel doping, multiple supply

voltage, and dual supply SRAMs [6]. The SRAM cell operates in three modes: read, write, and hold, and the amount of leakage power it produces depends on the supply voltage, leakage current, and threshold voltage parameters [11]. The above-mentioned values altered depending on the mode of operation, indicating a better technique to lower the cell's power dissipation.

In the hold mode operation of a 6T SRAM cell, the stored digital logic values at nodes Q and QB are maintained due to the cross-coupled positive feedback inverter pair. In hold mode, the bottom NMOS transistor is operating in the subthreshold region and there is a leakage current flowing from stored node (Q or QB) to ground [16]. The data loss can occur due to this leakage path and the data may be flipped. as shown in above Fig. 2, an extra NMOS transistor is added between the inverter pair's pull-down NMOS transistors and ground to prevent leakage current and minimize static power loss in hold mode. The 7T SRAM Cell's word line signal regulates this additional NMOS transistor [7].

IV. SIMULATION RESULTS

The designed 6T and 7T schematics are shown below Fig 3 and Fig 4 using 45nm Technology. A Novel 7T SRAM cell is one of the best which dissipates very less amount of power during its operation. The simulation results are obtained in the cadence virtuoso tool at 45nm, when 6T is compared to 7T the power dissipation reduces as shown in the table. Because WL is zero in 6T during hold mode, leakage currents result in excessive power dissipation, however, in 7T we add an NMOS transistor to the inverter connection, which functions as a virtual ground during hold mode. As a result, the reverse currents are low, and the power dissipation is reduced. Furthermore, the novel 7T SRAM cell architecture showed enhanced performance in the presence of procedure variations, which makes it a potential solution for high-density memory applications.

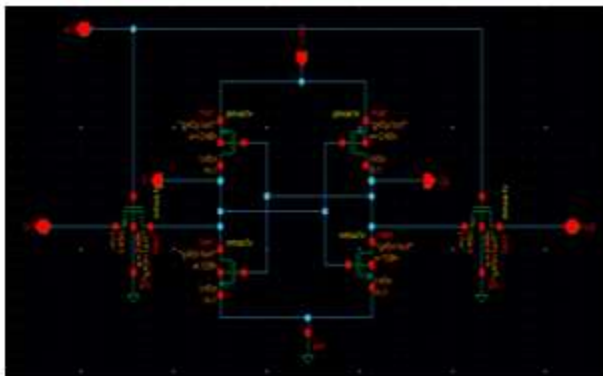

Fig 3: 6T SRAM cell schematic

Fig 4: 7T SRAM cell schematic

Fig 5: Comparison of Power Dissipation Between 6T and 7T SRAM cell

Power Dissipation in µ Watts		
VDD (V)	6T	7T
5	760	187
4	81.16	70.12
3	45.34	27.3
2	33.85	20.11
1	25.44	15.35

Table 1: Power Dissipation

45 nm Technology		
	6T	7T
SNM (mv)	293.46	264.67

Table 2: Static Noise Margin

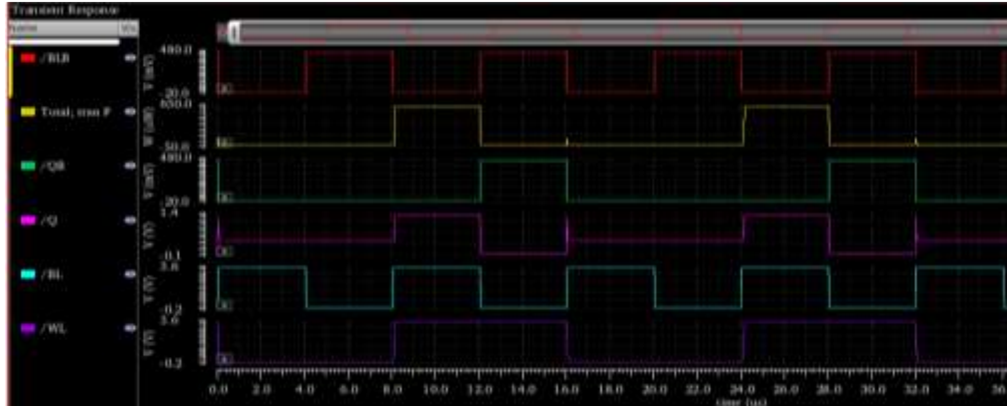

Fig 6: Output wave form of 7T SRAM cell

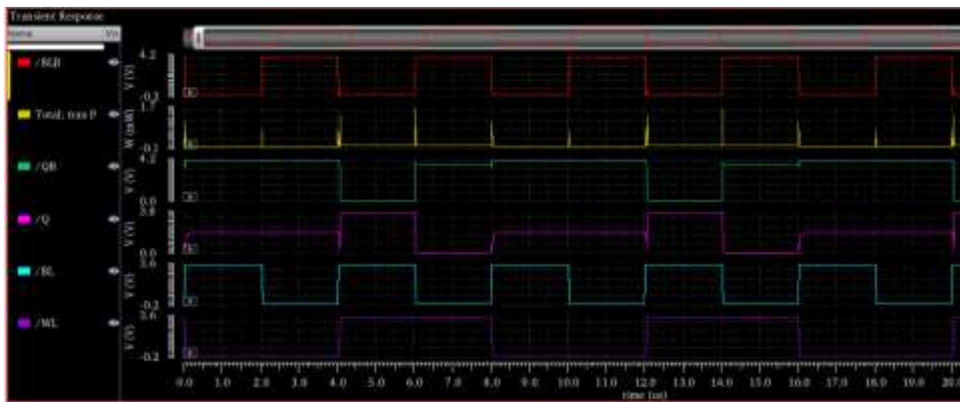

Fig 7: Output wave form 7T SRAM cell

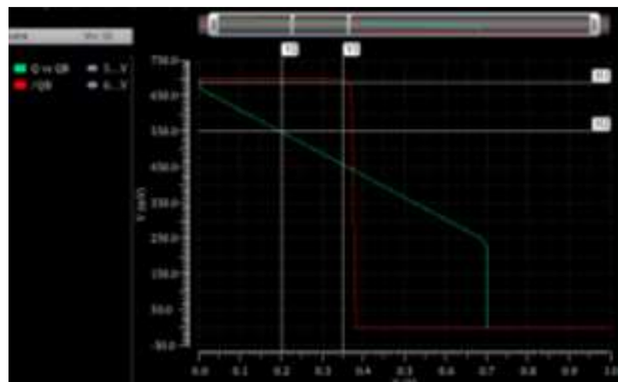

Fig 8: Static Noise Margin

The stability of the SRAM is also a major part in the memory cell, if the memory is stable then the data inside is stable and safe. But in 7T SRAM cell stability is less compared to 6T SRAM cell, the stability of the cell depends on the SNM as shown in the above Table 2 and the Fig 8 represents the SNM output shown in butterfly curve. The compared power dissipation of 6T and 7T are shown in Table 1 and Fig 5 as graphical. It has the lowest power dissipation compared to 6T and it almost saves 75% of power dissipation at 5V and 60% of power dissipation at 1V which means only 5% is decreased but compared

to 6T it dissipates very less. Also, we can observe the output wave forms of the 7T SRAM cell in the Fig 6 and Fig 7.

V. CONCLUSION

The proposed 7T SRAM cell architecture presents an innovative solution to address the challenges associated with the conventional 6T SRAM cell. The proposed architecture utilizes a feedback loop, along with a combination of NMOS and PMOS transistors, to maintain stability during read and write operations. Simulations show that the proposed architecture has significant improvements in stability margins and power consumption, as well as a higher tolerance to process variations. As such, it has the potential to enhance the performance of future digital systems.

Going forward, further research and optimization of the proposed 7T SRAM cell architecture will be required before implementing it into real-world applications. However, the results of this study show that the 7T SRAM cell architecture is a promising development that can overcome the limitations of the conventional 6T SRAM cell. Overall, the proposed architecture has the potential to improve stability margins, reduce power consumption, and enhance the tolerance to process variations, making it an ideal solution for high-density memory applications.

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