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DESIGN OF LOW POWER BASED CARRY LOOK AHEAD ADDER USING DOMINO LOGIC FOR HIGH SPEED ALU APPLICATION

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ABSTRACT

Built-In Self-Test (BIST) is a technique that allows a set up to check itself for any error on its own. BIST is a screening mechanism that places the testing functions physically with the circuit under test (CUT). BIST can make the system-level design process much simpler in essential applications where system reliability is predominant, and “failure is not an option.” The decision to execute a critical mission must be made only if the complete system is running without any error. BIST structures generate pseudo random combinations and output results for an exclusive circuit under test are compared. BIST can be implemented on entire designs, design blocks or structures within design blocks. Memory is a complex architecture (fabrication wise) and used in a large number of applications. BIST is basically used to help in the testing of memory with the help of a few extra pins. In fact, while testing a memory using BIST, applying a simple clock signal along with a few pins helps test the entire memory IC.

1. INTRODUCTION

Although the standard-cells based design is often called full custom design, in a strict sense, it is somewhat less than fully custom since the cells are pre-designed for general use and the same cells are utilized in many different chip designs. In a fuller custom design, the entire mask design is done anew without use of any library. However, the development cost of such a design style is becoming prohibitively high. Thus, the concept of design reuse is becoming popular in order to reduce design cycle time and development cost. The most rigorous full custom design can be the design of a memory cell, be it static or dynamic. Since the same layout design is replicated, there would not be any alternative to high density memory chip design. For logic chip design, a good compromise can be achieved by using a combination of different design styles on the same chip, such as standard cells, data-path cells and PLAs. In real full-custom layout in which the geometry, orientation and placement of every transistor is done individually by the designer, design productivity is usually very low - typically 10 to 20 transistors per day, per designerin digital CMOS VLSI, full-custom design is rarely used due to the high labor cost. Exceptions to this include the design of high-volume products such as memory chips, high-performance microprocessors and FPGA masters. The full layout of the Intel 486 microprocessor chip, which is a good example for a hybrid full-custom design.THE aggressive scaling of microelectronic technology is enabling the fabrication of increasingly complex

ICs. Together with several benefits (improved performance, decreased cost per function, etc.), this poses serious challenges in terms of test and reliability In particular, during at-speed test of high-performance microprocessors, the IC activity factor (AF) induced by the applied test vectors is significantly higher than that experienced during in field operation Consequently, excessive power droop (PD) may be generated, which will slow down the circuit under test (CUT) signal transitions. This phenomenon is likely to be erroneously recognized as due to delay faultsas a result, a false test fail will be generated, with consequent increase in yield loss At-speed test of logic blocks is nowadays frequently performed using MBIST (MBIST) which can take the form of either combinational MBIST or scan-based MBIST, depending on whether the CUT is a combinational circuit or a sequential one with scan. In case of scan-based MBIST, two basic capture-clocking schemes exist the launch-on-capture (LOC) scheme. In LOS schemes, test vectors are applied to the CUT at the last clock (CK) of the shift phase, and the CUT response is sampled on the scan chains at the following capture CK. In the LOC scheme, instead, test vectors are first loaded into the scan-chains during the shift phase; then, in a following capture phase, they are first applied to the CUT at a launch CK, and the CUT response is captured on the scan chains in a following capture CK [8]. In this paper, we consider the case of sequential CUTs with scan-based MBIST adopting a LOC scheme, which is frequently adopted for high-performance microprocessors. They suffer from the PD problems discussed above, especially during the capture phase, due to the high AF of the CUT induced by the applied test patterns. Solutions allowing designers to reduce PD during the capture phase in scan-based MBIST are therefore needed. While several approaches have been proposed to reduce PD for combinational MBIST PD is reduced by a multicycle BIST scheme with partial observation. This approach does not impact on fault coverage (FC) (actually, it presents a slight FC increase of 5% compared with conventional scan-based-MBIST), but enables reduction of PD by 33% only, compared with conventional scan-based-MBIST. In , PD can be reduced by more than 50% by alternately disabling groups of scan chains during test. However, this approach implies an increase of more than 90% in the number of test vectors required to achieve a target FC, with consequent increase in test time (TT), compared with conventional scan based MBIST. In a test pattern generator with a preselected toggling level is presented. It enables more than 50% reduction in the AF of the scan chains by preselecting the number of shift cycles during which the scan chains are loaded with constant logic values. However, it requires more than 60% increase in the number of test vectors (thus TT) to achieve the same FC as with conventional scan-based MBIST. The solution in relies on inserting an additional phase, namely a burst phase, between each shift and capture phase. Such a burst phase aims at increasing the current drawn from the power supply, up to a value similar to that absorbed by the CUT during capture phases. This way, the inductive component of PD occurs during the burst phase, and vanishes before the following capture phase. This solution causes an increase in both the total power consumed during test and TT. Omaña et al. [recently proposed

alternative approaches to reduce PD during scan-based MBIST, for the LOS scheme. They enable reduction of PD (up to 50% in , and up to 87% in by increasing the correlation between adjacent bits of the scan chains. However, these approaches do not increase the correlation between test vectors applied at the following capture cycles, so that they are not effective in reducing PD during scan-based MBIST adopting the LOC scheme. In this paper, we propose a novel, scalable approach to reduce PD during capture phases of scan-based MBIST, thus reducing the probability to generate false test fails during test. Similar to the solutions in and, our approach reduces the AF of the CUT compared with conventional scan-based MBIST, by properly modifying the test vectors generated by the Linear Feedback Shift Register (LFSR). Our approach is somehow similar to reseeding techniques (e.g., that in to the extent that the sequence of test vectors is properly modified in order to fulfill a given requirement that, however, is not to increase FC (as it is usually the case for reseeding), but to reduce PD. The basic idea behind our approach (in its non-scalable version) was introduced in .In our proposed scalable approach, one (or more) test vector(s) to be applied to the CUT according to conventional scan based MBIST is (are) replaced by new, proper test vector(s), hereinafter referred to as substitute test (ST) vector(s). The ST vector(s) is (are) generated based on the test vectors to be applied at previous and future capture phases in order to reduce the maximum number of transitions between any two following test vectors. This way, the CUT AF and PD are reduced compared with the original test sequence . We consider the presence of a phase shifter (PS), which is usually adopted in scan-based MBIST to reduce the correlation among the test vectors applied to adjacent scan-chains. As shown in , all test vectors to be applied at previous and future capture phases to any scan-chain are usually given at proper outputs of the PS, or the PS can be easily modified to provide them. In our approach, this property is exploited to enable its low-cost hardware implementation. However, our approach can also be adopted if the PS does not provide the previous and future test vectors for all scan-chains or if the scan-based MBIST does not present a PS. Indeed, as shown in Section IV, the previous and future test vectors of scan-chains can be obtained as a linear combination of proper LFSR outputs. Our approach is scalable in the achievable PD reduction.

2. LITERARTURE SURVEY

Scan flip flops, especially, the ones close to the scan-in pins, are not observable in most of shift cycles. Tsai et al. [1] proposed a novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the earlier work, presented in [2], selects different numbers of capture cycles after the shift cycles. In this paper, a new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. Weighted pseudorandom testing schemes [3] can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test

pattern generation scheme was proposed for scan-based BIST in , according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. A reconfigurable scan architecture was used for the deterministic BIST scheme in using the weighted test enable signal-based pseudorandom test generation scheme. Lai et al. proposed a new scan segmentation approach for more effective BIST. LP BIST approaches were proposed early in [4].Zorian [5] proposed a distributed BIST control scheme in order to simplify the BIST execution of complex ICs. The average power was reduced and the temperature was reduced. The methods reduced switching activity during scan shifts by adding extra logic [6]. A new random single-input change test generation scheme in generates LP test patterns that provide a high level of defect coverage during LP BIST of digital circuits. An LP BIST scheme was proposed based on circuit partitioning [7]. New pseudorandom test generators were proposed to reduce power consumption during testing A new encoding scheme is proposed in [8], which can be used in conjunction with any LFSR-reseeding scheme to significantly reduce test power and even further reduce test data volume. Lai et al. [9] proposed a new LP PRPG for scan-based BIST using a restricted scan chain reordering method to recover the fault coverage loss. A low-transition test pattern generator in [10] was proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions: 1) between consecutive patterns and 2) between consecutive bits. Abu-Issa and Quigley [11] proposed a PRPG to generate test vectors for test-per-scan BISTs in order to reduce the switching activity while shifting test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. A new adaptive low shift power pseudorandom test pattern generator was presented in [12] to improve the tradeoff between test coverage loss and shift power reduction in MBIST. This is achieved by applying the information derived from test responses to dynamically adjust the correlation among adjacent test stimulus bits. Filipek et al. [13] and Solecki et al. A novel low-power BIST technology was proposed in that reduces shift power by eliminating the specified high frequency parts of vectors and also reduces capture power. Multicycle tests support test compaction by allowing each test to detect more target faults. The ability of multicycle broadside tests to provide test compaction depends on the ability of primary input sequences to take the circuit between pairs of states that are useful for detecting target faults. This ability can be enhanced by adding DFT logic that allows states to be complemented in [14]. A new DFT scheme for launch-on-shift testing was proposed in [39], which ensures that the combinational logic remains undisturbed between the interleaved capture phases, providing computer-aided-design tools with extra search space for minimizing launch-to-capture switching activity through test pattern ordering. Complete fault coverage can be obtained [15] when the pseudorandom test generator is modified. A combination of a pseudorandom test generator and a combinational mapping logic was constructed by Chatterjee and Pradhan to produce a given target pattern set of the hard-to-detect faults.

3. EXISTING SYSTEM

Several methods exist for testing manufactured ICs (i.e. the proper detection of faulty IC amongst all manufactured ICs with minimal 'defect level'). The DFT require an additional hardware which help in reducing test generation complexity as well as reducing test application cost. Today most of the systems are designed with integrated test strategy such as BIST which utilizes on chip extra hardware. The BIST replaces the traditionally used automatic test equipment (ATE) to offer several advantages over ATE. Generally, the ATE cost increases for higher tester pin count and also its inability for higher clock rates (i.e. more than 1GHz) due to pin inductance. The BIST is used to test generally the embedded memories such as RAM and Cache . There are several test algorithms which help to detect different types of faults possible in the memories. These faults are single stuck-at fault (SAF), address decoder fault (AF), transition fault (TF), inversion coupling fault (CFin), idempotent coupling fault (CFid), dynamic coupling fault (CFdyn), state coupling fault (SCF) etc.

4. PROPOSED SYSTEM

The design technique, technique, BIST, is used to test the circuit itself using some parts of the same circuit. With properly designed BIST architecture the additional testing hardware expense will be very much balanced by the advantages in terms of enhanced reliability and minimized maintenance expense. BIST minimizes total cost by reducing test pattern creation attempts at all levels, minimizing testing work at chip, improving system level maintenance and enhancing component repair . Moreover, it can test numerous circuits simultaneously as well as minimized testing time is provided at operational real time clock. It reduces test-cycle duration. Every household appliance, computer, laptops uses memory chips. So BIST enabled memory ultimately helps everybody to serve better. The proposed work concentrates on the standard RAM chip design with BIST enabled architecture using linear feedback shift register (LFSR) with the help of Very High-Speed Integrated Circuit Hardware Description Language (VHDL). The fundamental BIST construction needs the inclusion of additional three h/w building blocks to a digital circuit with Circuit under test (CUT). They are i) A test pattern generator ii) A response analyzer and iii) A test controller as shown in Fig 1.

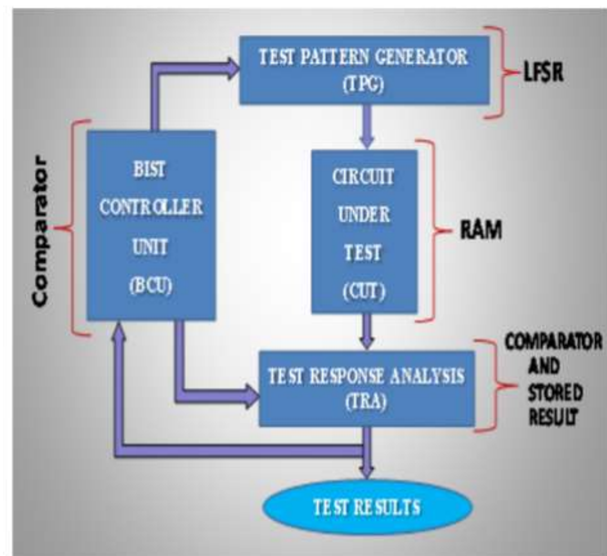

Fig 1: General BIST Construction

The test pattern generator creates the test patterns for the CUT. In standard way of exercise, the CUT accepts its inputs from other building blocks and execute the task for which it was planned. During test mode, pseudo random

test patterns are given to the CUT, and the output test results are evaluated by comparator. For the proposed work CUT is standard RAM, Test Pattern Generator (TPG) is implemented by simple LFSR, BIST Controller Unit (BCU) and Test Response Analyzer (TRA) is implemented by comparator.

CIRCUIT UNDER TEST(RAM) The main building block of the proposed work is standard RAM as shown in Fig. 2.

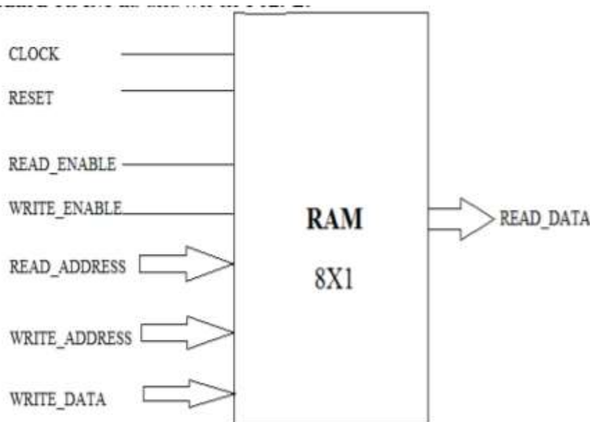

Fig. 2: RAM architecture block diagram

LFSR (BIT PATTERN GENERATOR)

LFSR (Linear Feedback Shift Register) is a combination of shift register and XOR gate. LFSR generally produces pseudorandom sequences. A pseudo-random binary sequence is basically an array of strings consisting of ‘0’s and ‘1’s which seems to be random in the appearance, but actually the sequence is repeated after some clock pulse according to design. LFSR is mainly a combination of a D-flip flop and a XOR gate. Here three LFSRs are used for three different working purposes. They are used for generating random sequences for write address, read address and write data. The block diagrams of the LFSRs and the pseudo random sequences are shown below. LFSR1: It is generating pseudo random sequences for read address that is going into ram when test mode is on.

BIST ENABLED RAM (FINAL PRODUCT)

As discussed, earlier BIST architecture need some extra pins to test the CUT. In this proposed work single extra pin named as check pin is used to enable the testability of the CUT as shown in Fig. 10. Check pin=0 indicates normal mode and check pin=1 indicates test mode. In normal mode the whole architecture will work as a normal RAM and READ_DATA output will not be compared with the stored output. In test mode RAM will accept the data from all three LFSRs and READ_DATA output will be compared with the expected stored output by comparator and BIST_OUTPUT will indicate the status of the RAM. The comparator compares the stored expected output with the read data and asserts the error signal (BIST_OUTPUT) when test mode is on. In normal mode comparison is not needed so the error signal will be disabled. Test mode and normal mode is differentiated with the help of three 2:1mux as shown in Fig. 3

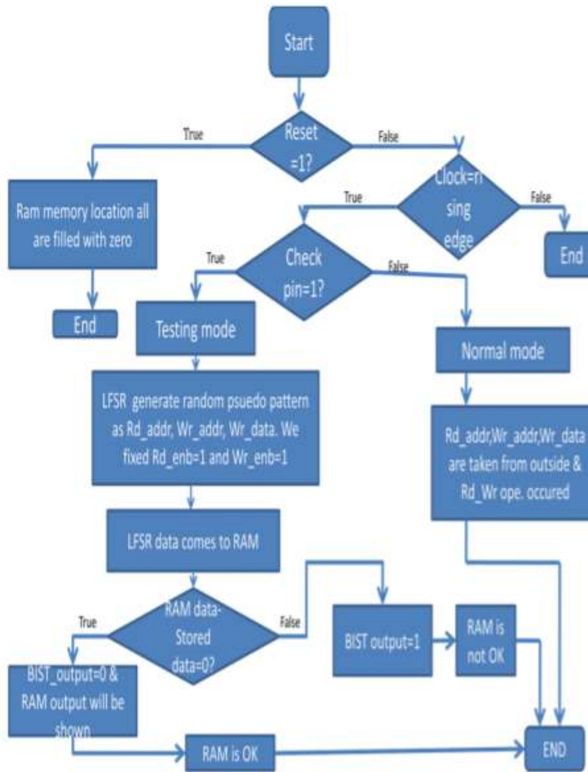

Fig. 3: Flow Chart of the final product

5. RESULTS

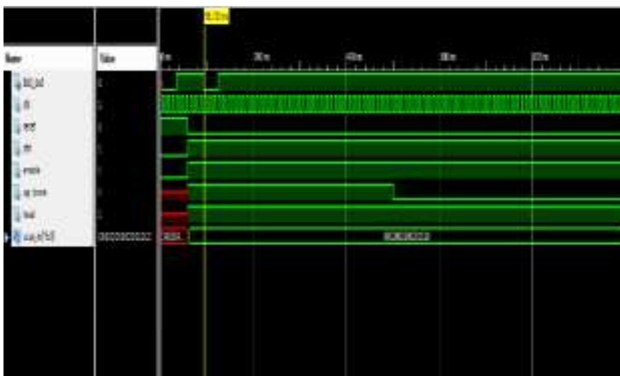

Fig. 4: Proposed simulation Results

Fig. 5: Power

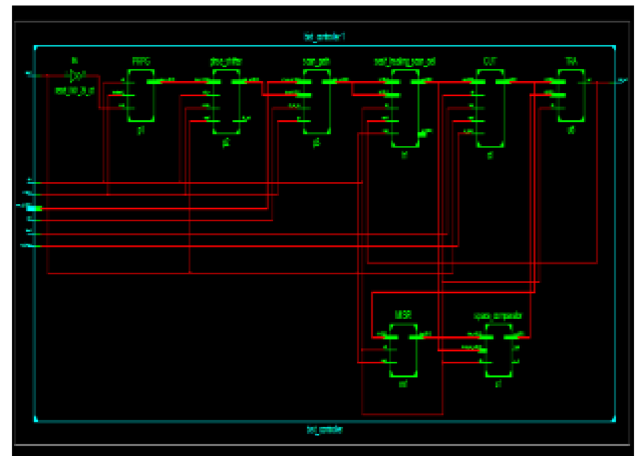

Fig. 6: proposed schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	513	607200	0%
Number of Slice LUTs	12142	303600	3%
Number of fully used LUT-FF pairs	348	12307	2%
Number of bonded IOBs	23	700	3%
Number of BUFG/BUFGCTRL/BUFHCEs	2	200	1%
Number of DSP48E1s	1	2800	0%

Fig. 7: Design summary

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================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:              0.511ns (Levels of Logic = 1)
  Source:            u6/out (FF)
  Destination:       bist_out (PAD)
  Source Clock:      clk rising

  Data Path: u6/out to bist_out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               1   0.232   0.279  u6/out (u6/out)
     OBUF:I->O                 0.000          bist_out_OBUF (bist_out)
    ----------------------------------------
    Total                      0.511ns (0.232ns logic, 0.279ns route)
                                       (45.4% logic, 54.6% route)

================================================================================
```

Fig. 8: Time summary

Table.1 Results comparison Table

Parameter	Existing Model	Proposed Model
Area	High	Arduino
Speed	Low	High
Power Consumption	High	Low
Efficiency	LOW	HIGH

6. CONCLUSION

In this paper we have presented memory BIST architecture and discussed about various blocks present in memory BIST. The controller algorithm for ‘MARCH C-’, ‘MARCH A’ and ‘MARCH Y’ and their Verilog implementation modelling and synthesis are compared. From the Algorithm description and synthesis results it is evident that ‘MARCH A’ algorithm is having more number of states and therefore controller implemented using ‘MARCH A’ occupies more area, consume more average power and still slower, while the controller implementation using ‘MARCH Y’ require least number of states and therefore it is occupies least area, consumes least power and yet bit faster. MARCH C-’ covers additional faults as compared to the ‘MARCH Y’ algorithm at the cost of little increase in the area, average power consumption and delay.

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